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Design Procedure for Millimeter-Wave InP DHBT Stacked Power Amplifiers

M. Squartecchia, T. K. Johansen, V. Midili

Technical University of Denmark, 2800 Lyngby

III-V Lab, 91120 Palaiseau, France

DTU Electrical Engineering
Department of Electrical Engineering

Outline

- Background and Motivation
- Technology
- Stacked Transistors Configuration
- Procedure for Power Cell Design
- Preliminary Results
  - Proof of concept
  - Implementation
- Conclusions

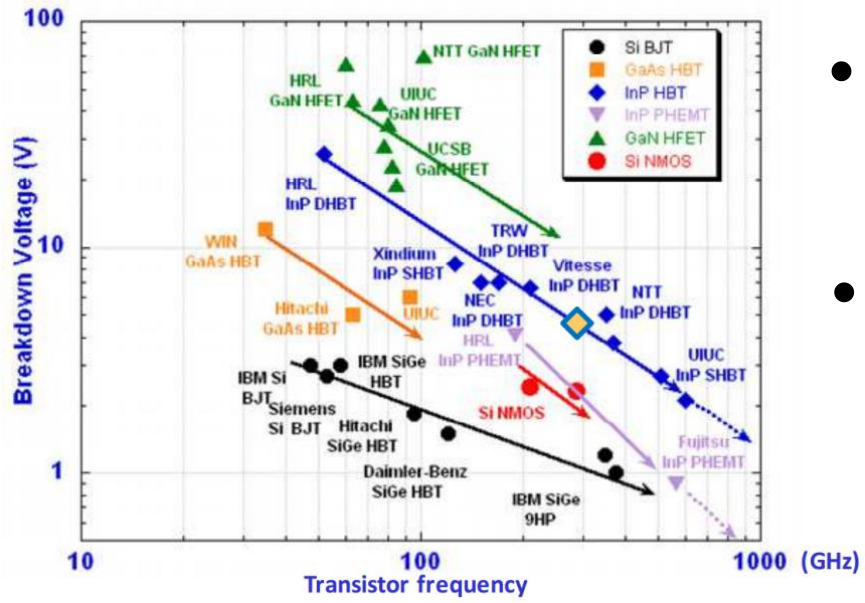
Background and Motivation

- **Wireless communications are increasingly taking place at E-band (71-76 GHz, 81-86 GHz) and higher millimeter-wave frequencies**
  - **Large absolute bandwidth**
  - **Low atmospheric attenuation**
  - **Small system size**

- **The main limitations are imposed by the power amplifier of the transmitter ($P_{Tx} \sim 1/f^2$)**

Background and Motivation

- **InP DHBT technology offers high frequency of operation and high density of integration with moderate breakdown voltage**



- **Geometrical downscaling**

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- **Breakdown voltage reduction**

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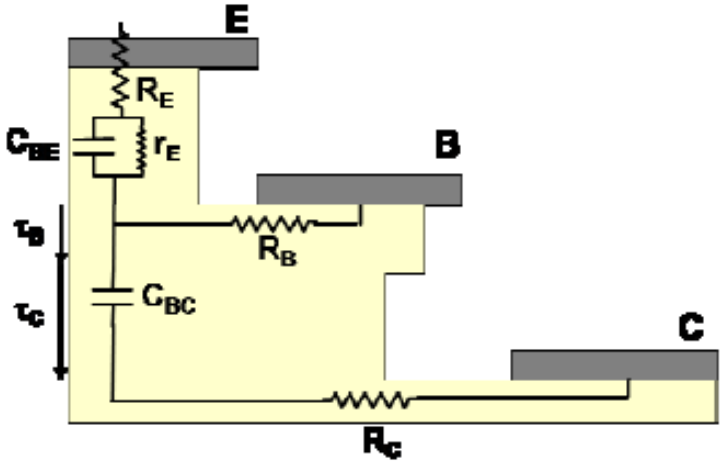
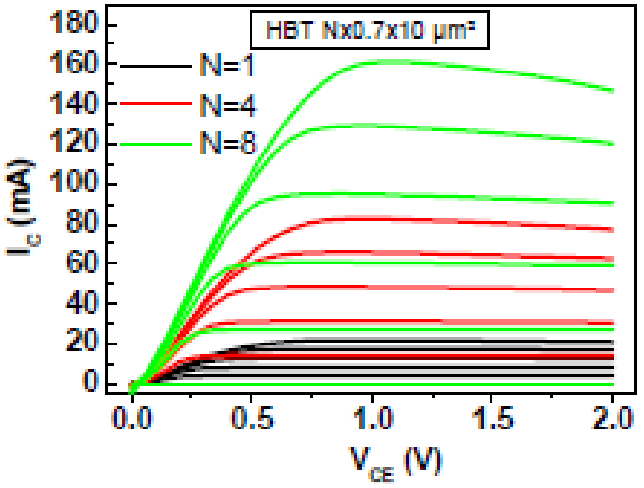
- **Investigation and design of new topologies**

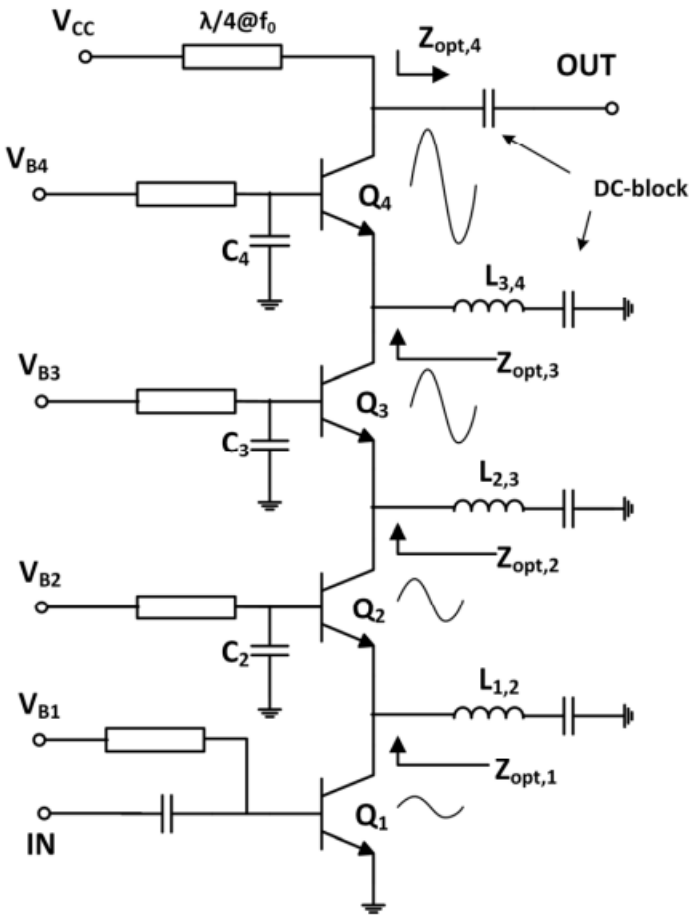
Technology

- **InP DHBT Technology developed at III-V Lab**
  - **1-finger device performances**
    β~40
    BV_{CE0}~ 4.9V
    f_T ~ 330 GHz
    f_{max} ~ 420 GHz
  - **4-finger device performances**
    f_T ~ 270 GHz
    Up to 360 GHz f_{max}
  - **4-finger HBTs with ballasting**
    Better « SOA »
    f_T~ 200 GHz
    f_{max}< 300 GHz





Stacked Transistors Configuration



- **Overall output voltage *n* times larger than a single device**
- **Current swing is the same**

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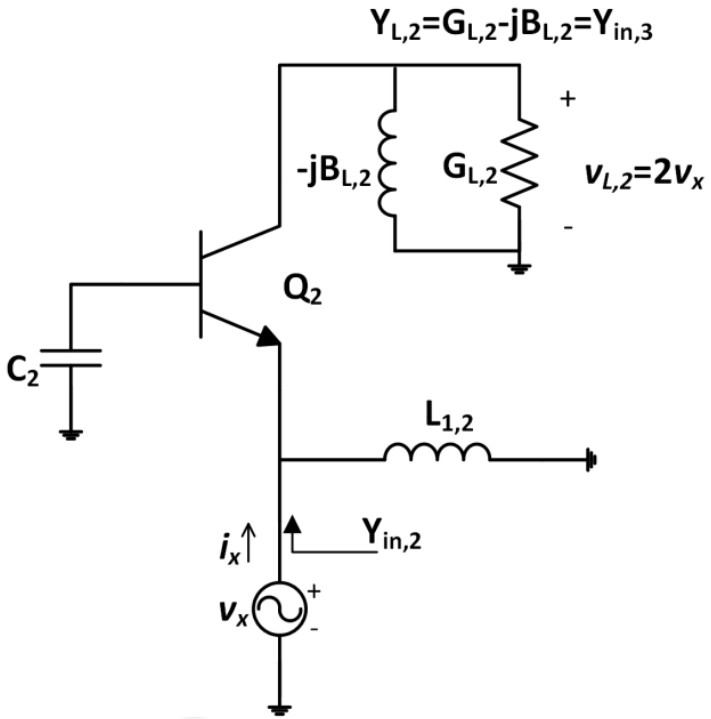
- **Output power n times higher**
- **Output voltage equally distributed among the devices**
- **Phase alignement required**

Procedure for Power Cell Design

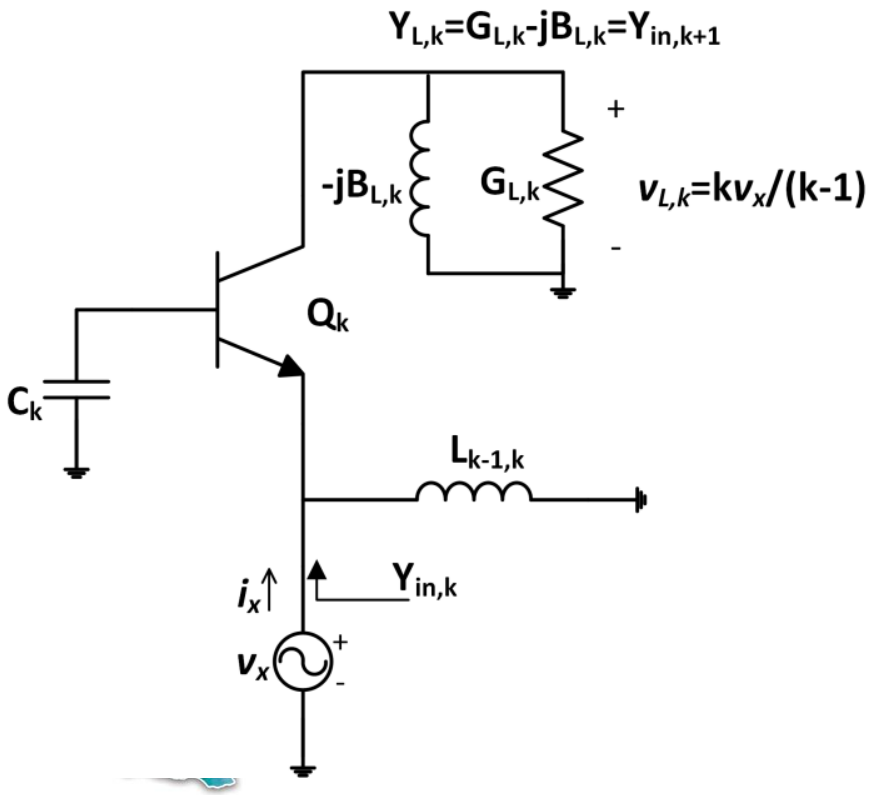
- **Nonlinear UCSD HBT model**
- **Load-Pull simulation for the common-emitter stage ($Z_{opt,1}$)**
- **The input impedance of the second stage must have the same value**

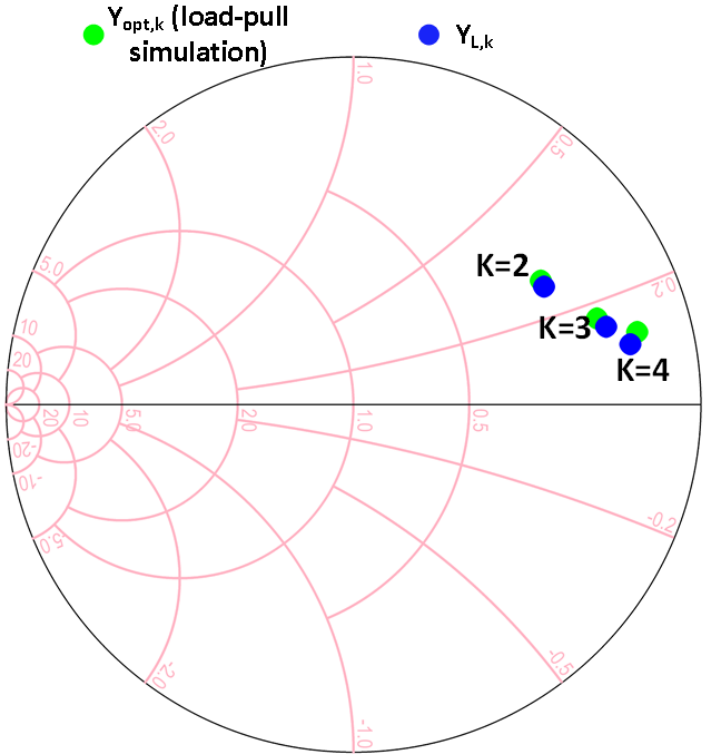


- $1/G_{L,2}=2\times \mathrm{Re}\{Z_{opt,1}\}$
- $B_{L,2}$ and C_2 for phase alignment and $\mathrm{Re}\{Y_{in,2}\}=\mathrm{Re}\{1/Z_{opt,1}\}$ (an adjustment on $G_{L,2}$ may be needed)
- $L_{1,2} \Rightarrow \mathrm{Im}\{Y_{in,2}\}=\mathrm{Im}\{1/Z_{opt,1}\}$

Procedure for Power Cell Design

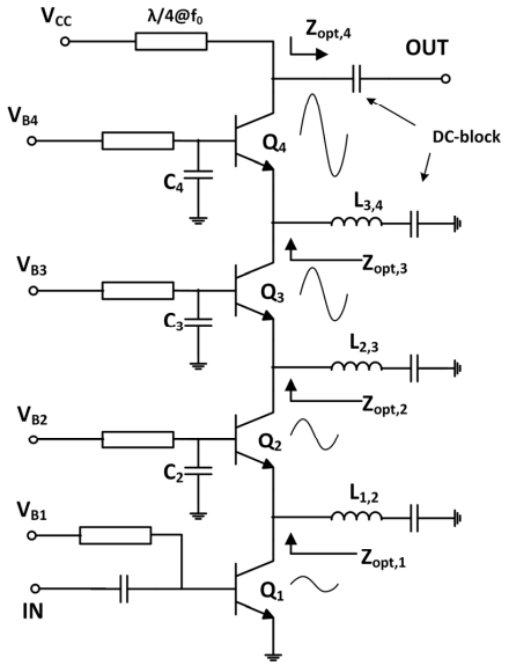
- The same procedure is repeated for the following stages
- Once $Y_{L,k}$ is found for the k-th stage, a load pull simulation can be performed on the k-transistor power cell to check if its value is close to the optimum



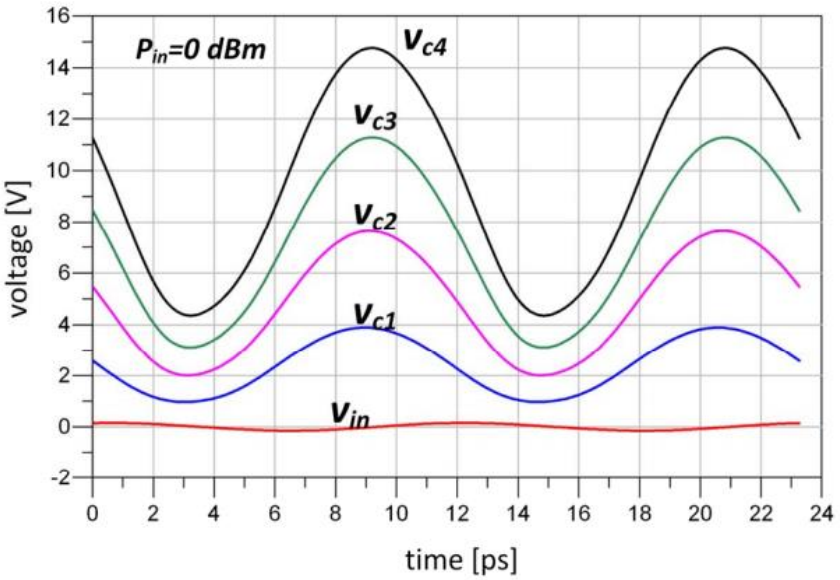


Preliminary Results (Proof of concept)

- **InP DHBT single finger devices**
  BV_{CE0}=4.9 V; f_T/f_{max}=330/420 GHz @ V_{ce}=2.4 V and I_c=15 mA



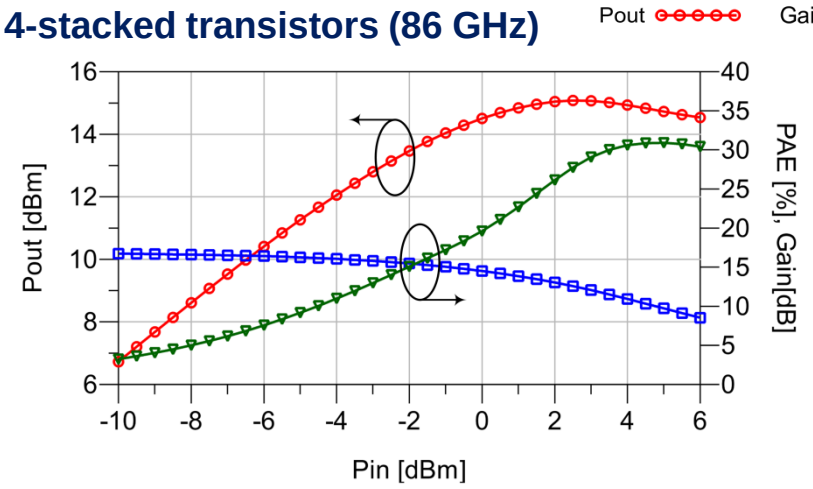
Collector waveforms at 1-dB compression point



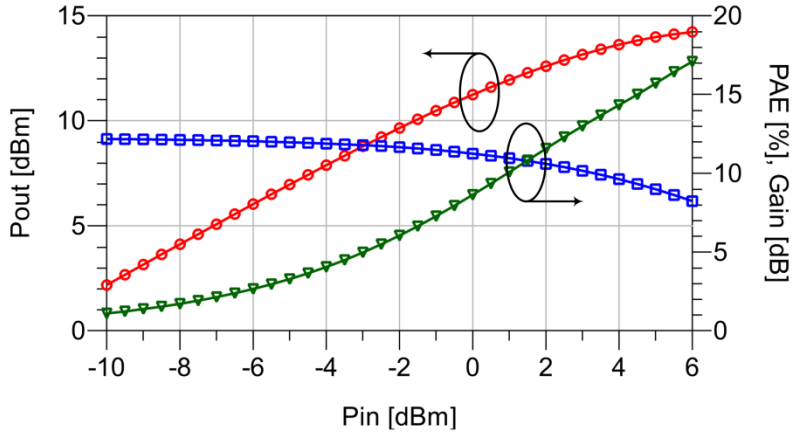
@ 86 GHz

Preliminary Results (Proof of concept)

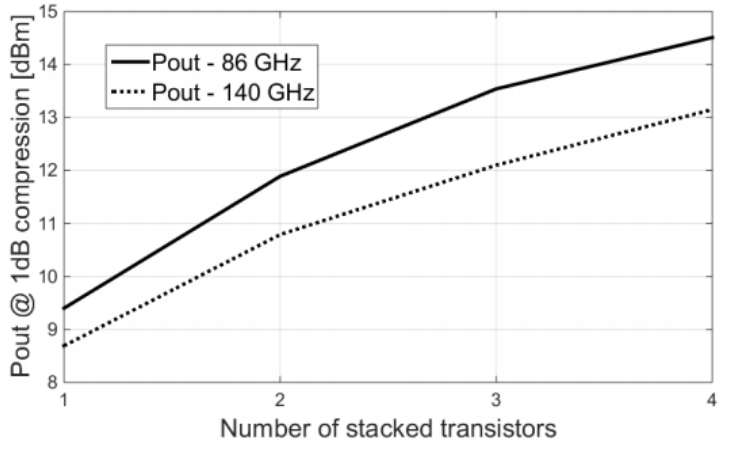
4-stacked transistors (86 GHz)



4-stacked transistors (140 GHz)

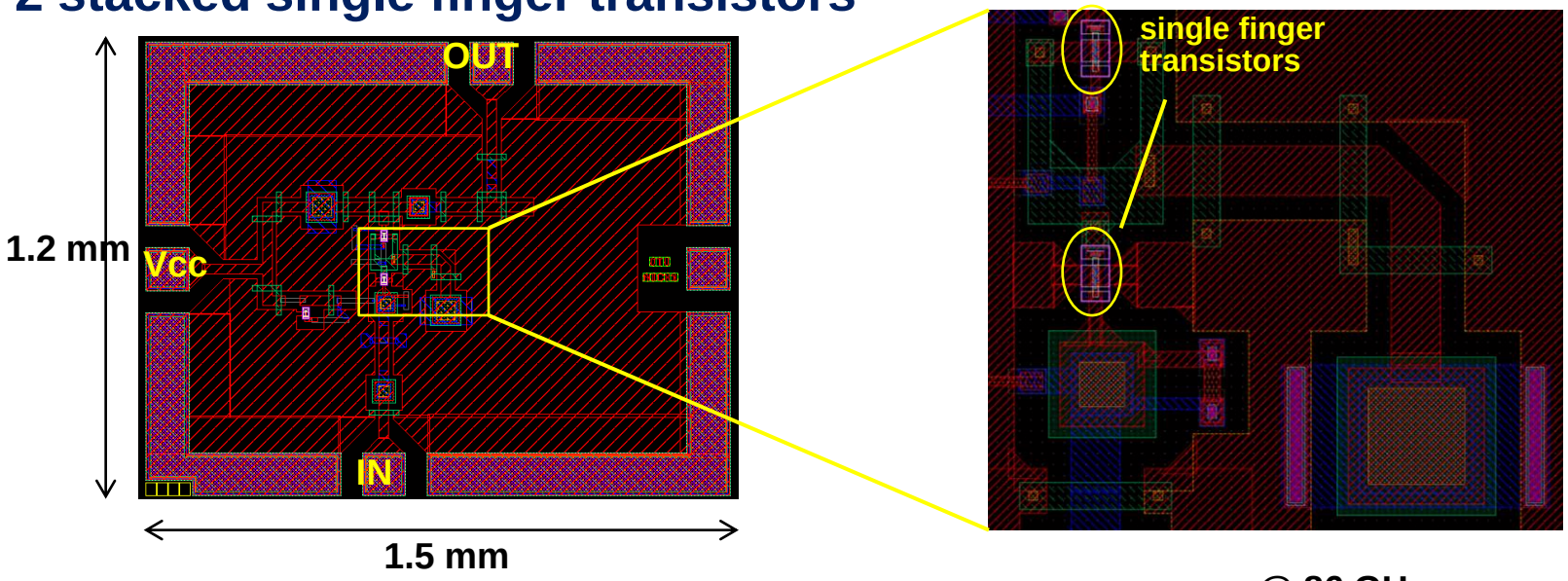


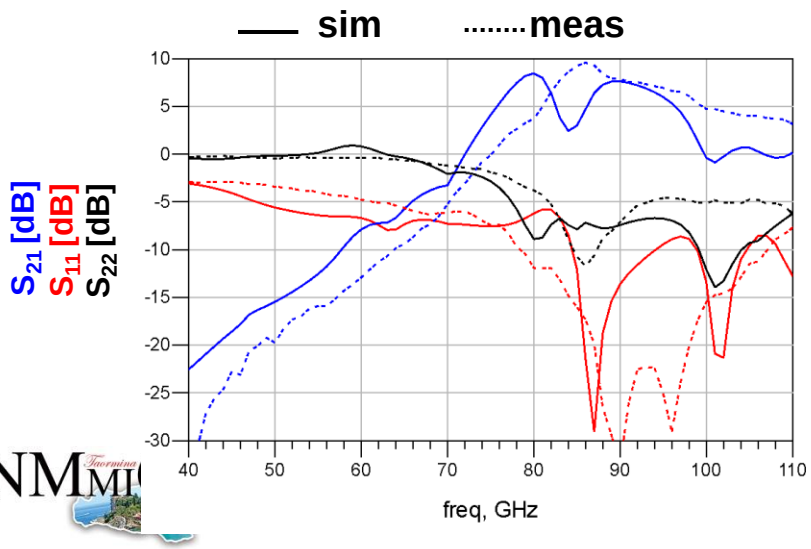
The design of the two- and three-stack power cells are intermediate steps for the design of the four-stack

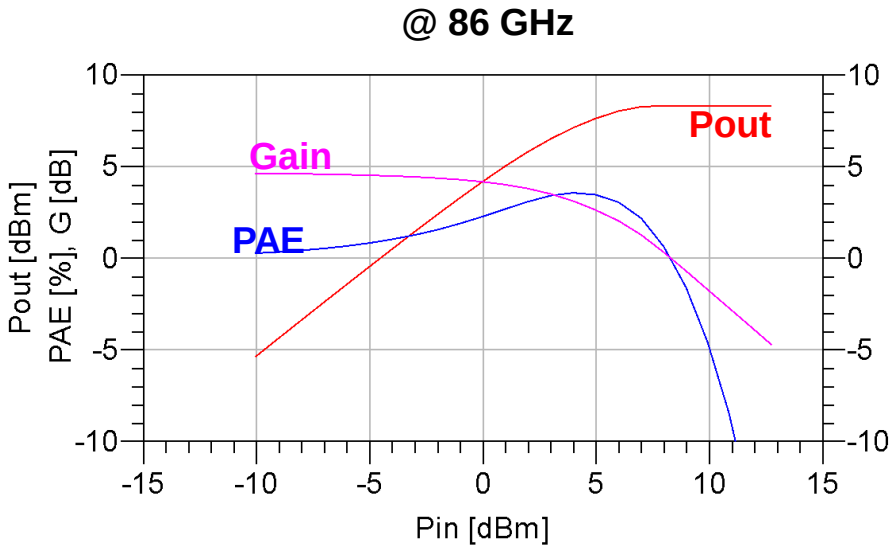


Preliminary Results (Implementation)

- **2 stacked single finger transistors**



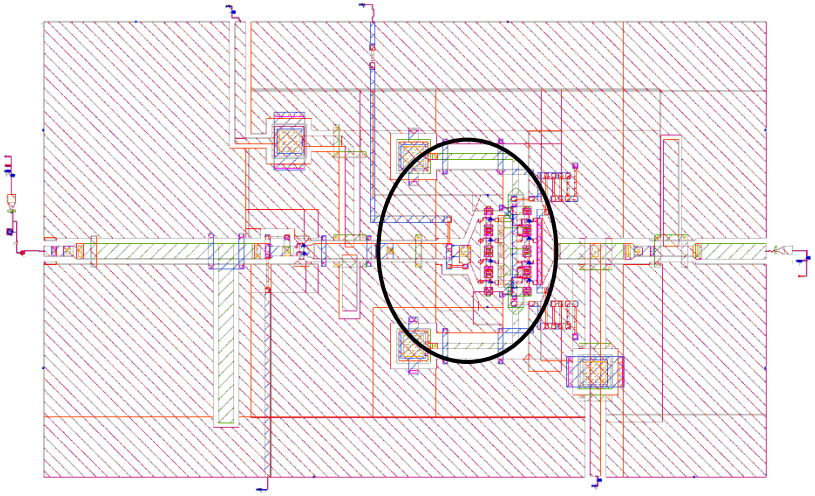




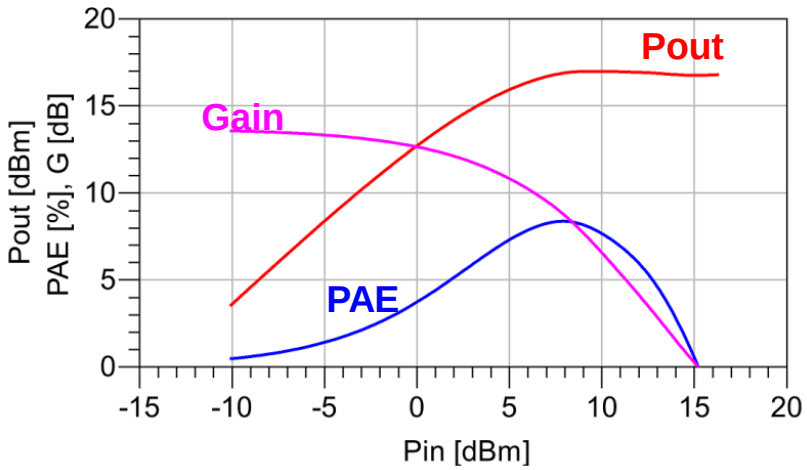
Preliminary Results (Implementation)

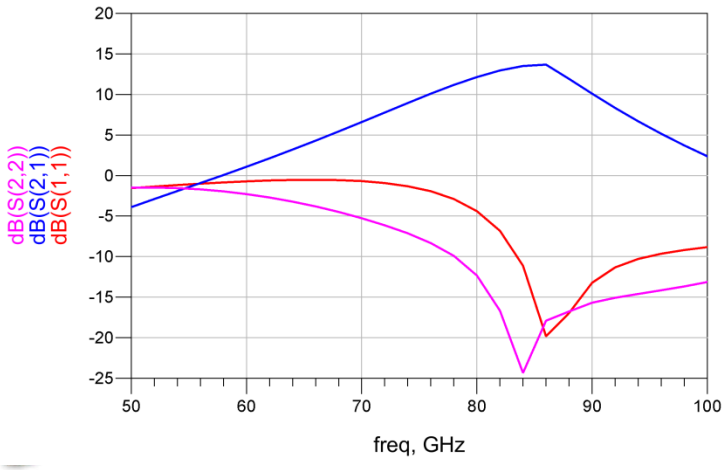
- **2 stacked ballasted four-finger transistors**

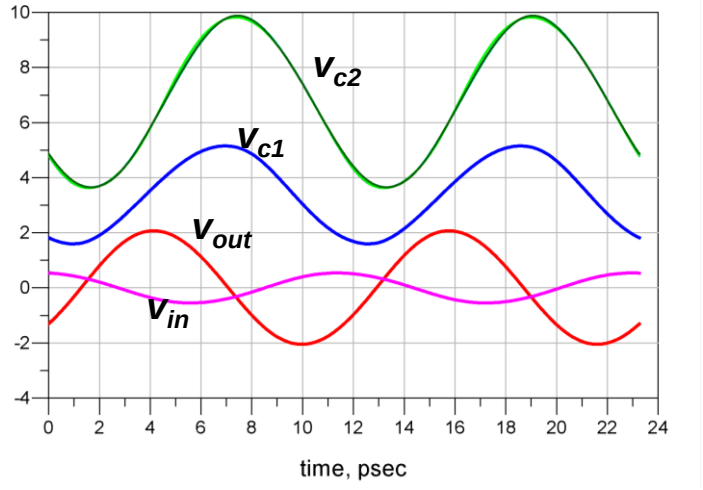
Electromagnetic-circuit co-simulation



@ 86 GHz







Conclusions

- **Possibility to apply the transistor-stacking concept to InP DHBT power amplifier operating at millimeter-wave frequencies**
- **An effective design procedure has been described and applied to two different four-transistor stacked power cells operating at 86 GHz and 140 GHz**

Perspectives

- **Realization of three- and four-stack power cells**
- **Investigation on efficient topologies for impedance matching**
- **Parallel combination of multiple power cells (e.g. Wilkinson, baluns...)**


III-V lab


European
Commission

Thank you for your attention!