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75 GHz InP DHBT Power Amplifier Based on Two-Stacked Transistors

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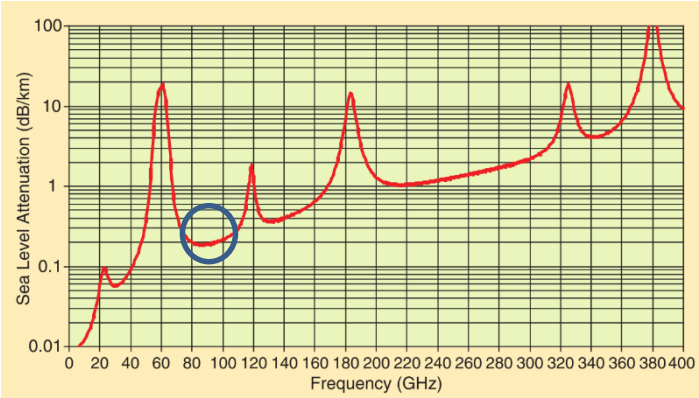
Outline

- Introduction and motivation
- Stacked-transistor configuration
- InP technology at III-V Lab
- Two-stacked transistor power cell
- Two-stage 8-way power amplifier
- Ongoing and future works
- Conclusions

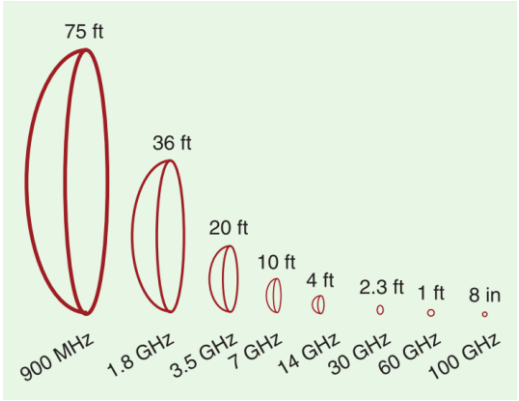
Introduction and motivation

- The W-band (75-110 GHz) has very favorable features

Low atmospheric attenuation



Small system size



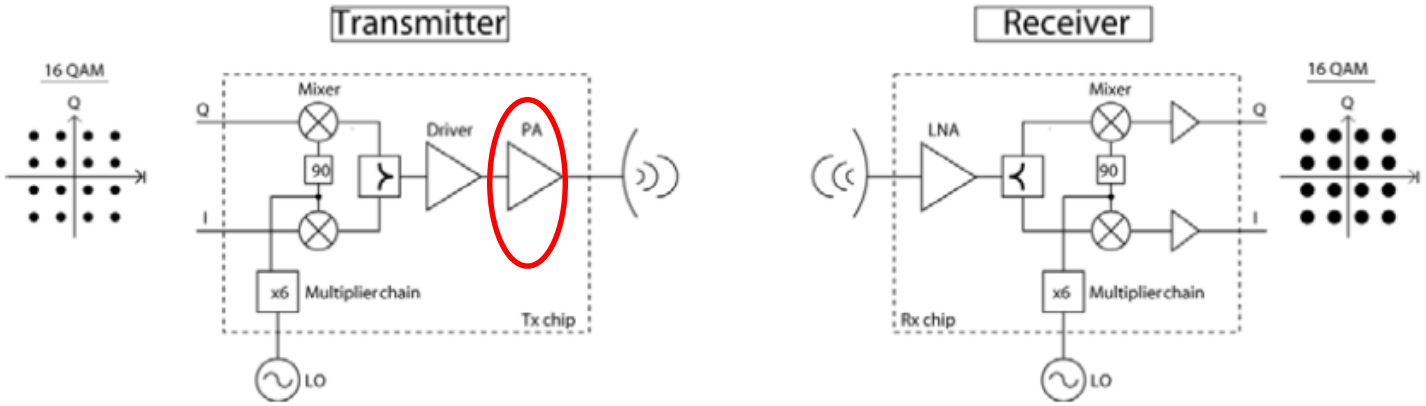
- Emerging applications:
  - Satellite and back-haul wireless links at E-band (71-76 GHz and 81-86 GHz)
  - Automotive radars (77 GHz)
  - Radio astronomy and earth observation (94 GHz)
  - .....

NEED FOR POWER AMPLIFIERS

Introduction and motivation

- W-band power amplifiers design challenges

  Ex: Wireless data link



1) High output power; 2) High gain; 3) Efficiency; 4) Good linearity

- High frequencies of operation → device downscaling → low breakdown voltages

$$\Rightarrow \quad P_{Tx} \cdot f^{2} \approx const$$

- Investigation on topologies to overcome these limitations

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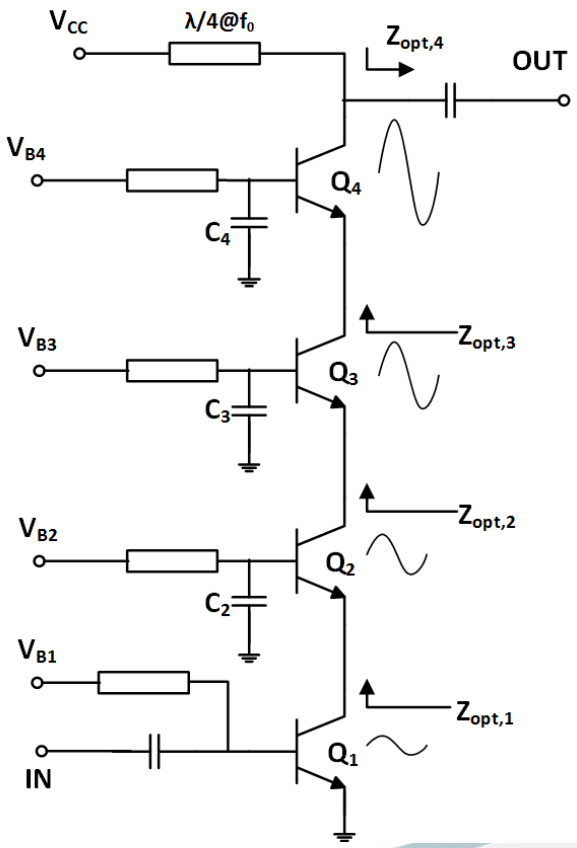
Stacked-transistor configuration



- The overall output voltage swing is *n* times higher than a single device
- Approximately the same current flows through all the transistors

⇩

- Output power and gain are potentially *n* times higher than a single device

- Design constraints:
  - Voltage equally shared
  - Phase alignment
  - Interstage matching

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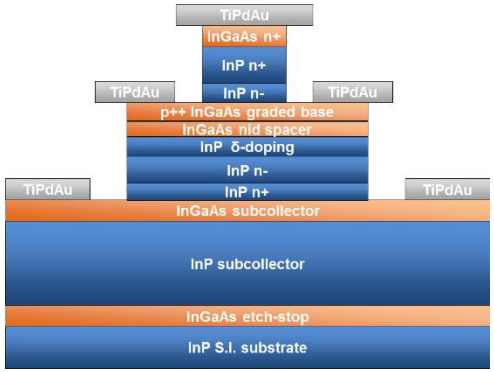
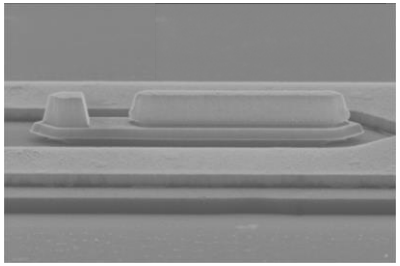
InP technology at III-V Lab

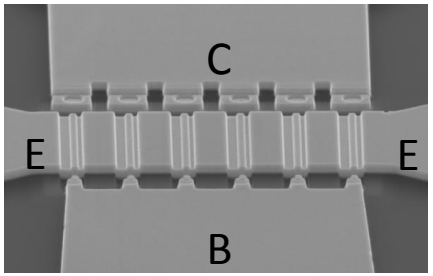
Double Heterojunction Bipolar Transistors (DHBTs)



Single-finger device



Multifinger device



Emitter width: W_E = 0.7 µm

Available emitter lengths: L_E = 5µm, 7µm and 10µm

High-speed mixed-signal optimized process (aka SHARC)

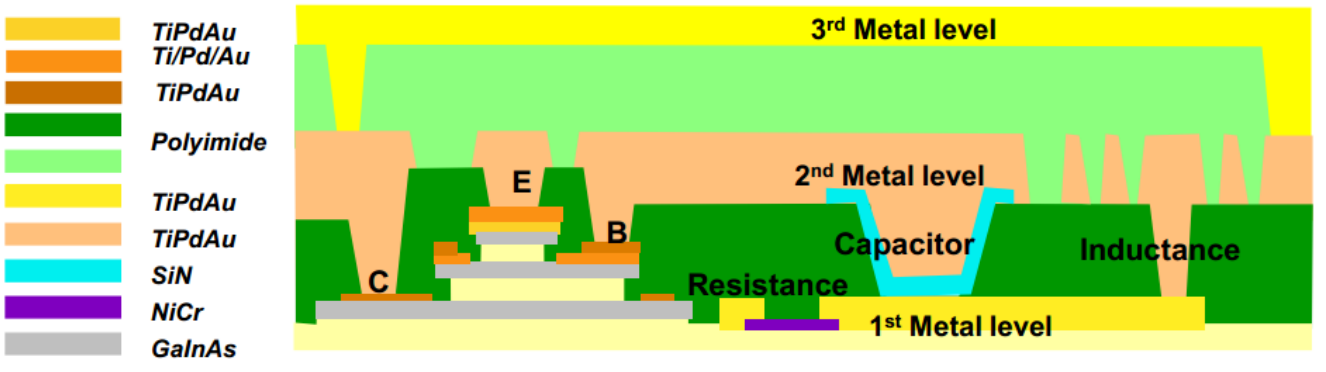
- β > 25
- f_T ≈ 400 GHz
- f_{max} > 350 GHz
- BVceo ≈ 5 V

Power optimized process (aka SAND)

- Thicker collector
- β > 25
- f_T ≈ 270 GHz
- f_{max} > 420 GHz
- BVceo ≈ 7 V

InP technology at III-V Lab

Layer stack



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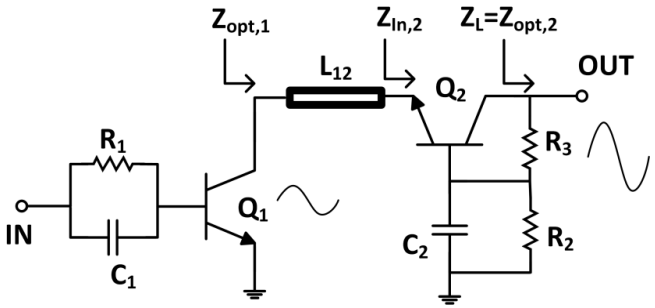
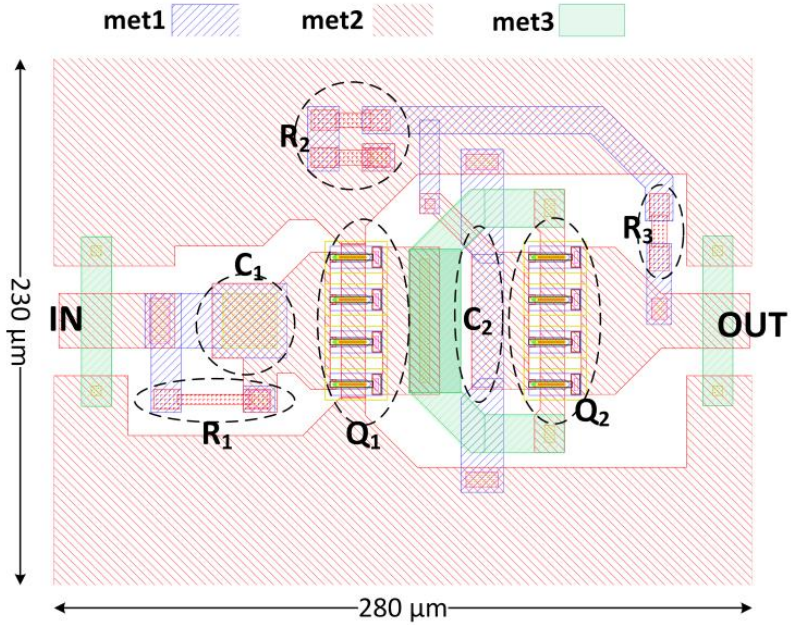
Two-stacked transistor power cell

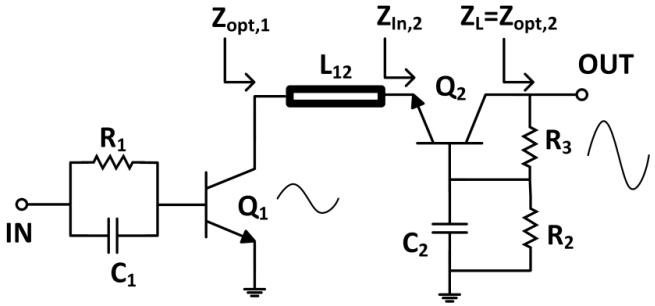




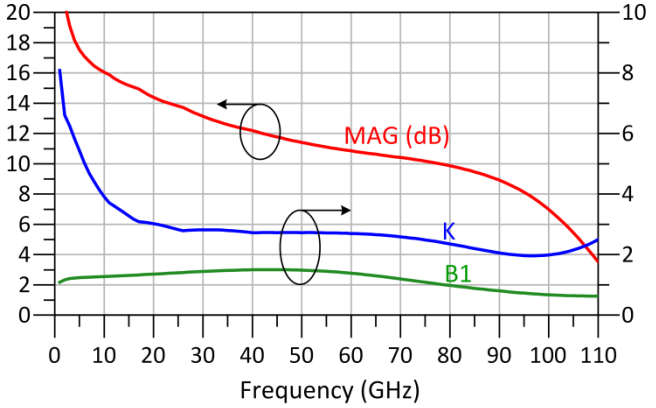
- Four-finger devices (4×0,7×10 µm^2)
- Q1-Q2 → UCSD model
- Class A: $V_{ce1}=V_{ce2}=2.4$ V and $I_{c1}\approx I_{c2}=60$mA
- R_1-C_1 for biasing and low frequency stability
- R_2-R_3 for self-bias and improved stability
- L_{12}: physical connection and interstage matching

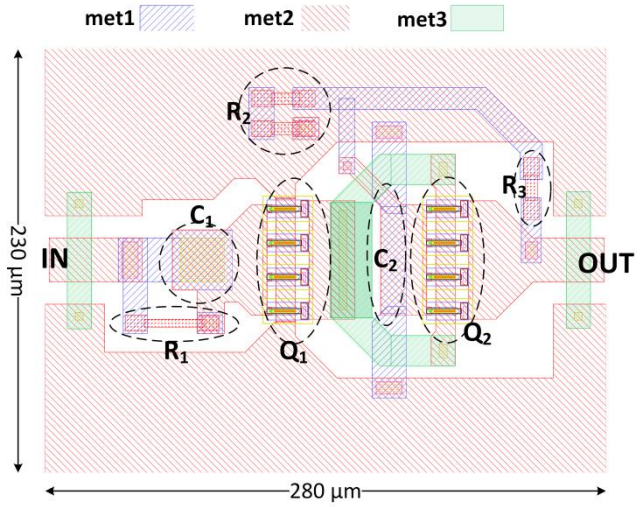
Two-stacked transistor power cell

EM-circuit co-simulation and optimization

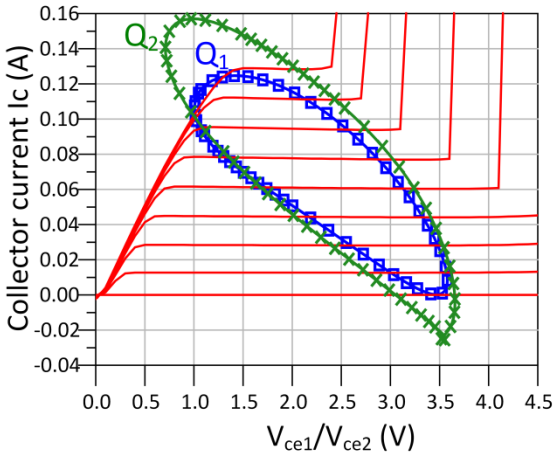


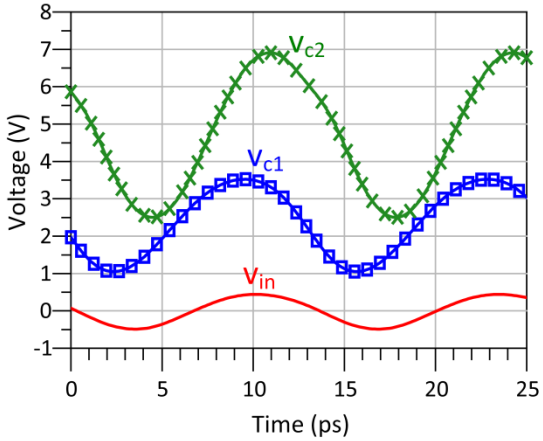
R_1=250 Ω
C_1=300 fF
C_2=80 fF
R_2=130 Ω
R_3=60 Ω





@ 75 GHz



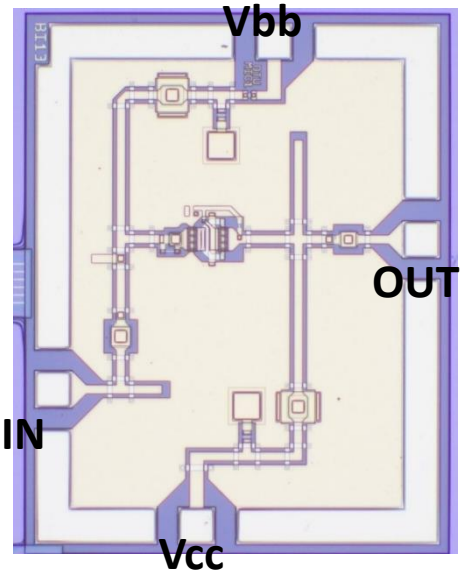


$Z_L=Z_{opt,2}\approx 14+j*8\ \Omega$ Pin≈10 dBm Pout≈18 dBm

Two-stacked transistor power cell

Matched power cell

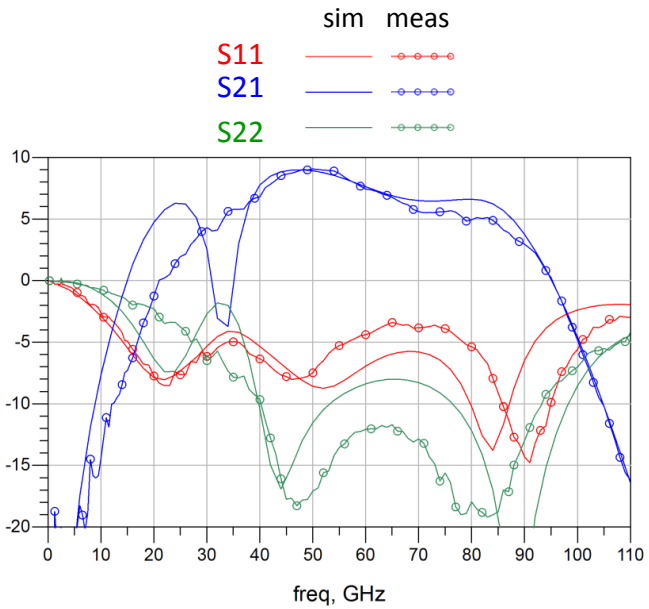
(SHARC process realization)



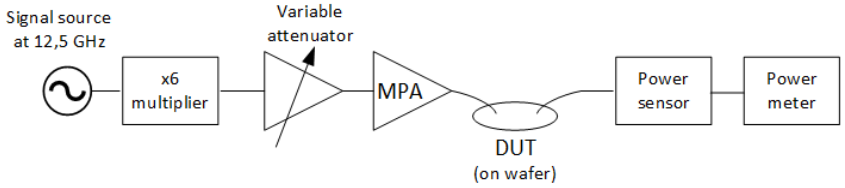
Bias settings

Vbb=1.4 V
Ibb=1.9 mA

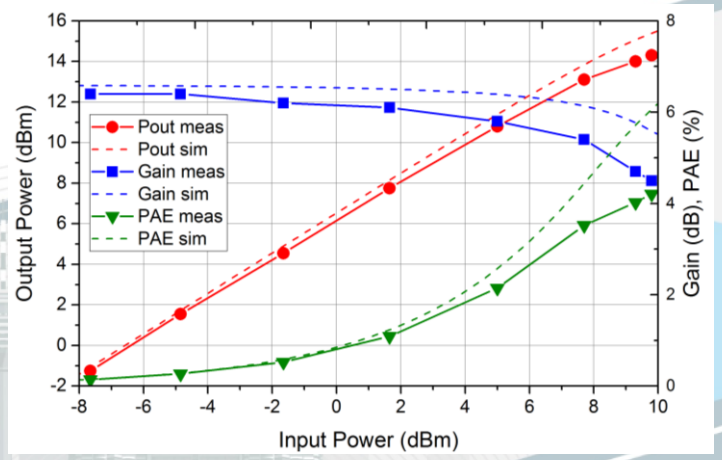
Vcc=4.9 V
Icc=84 mA



Power sweep measurement setup



81 GHz



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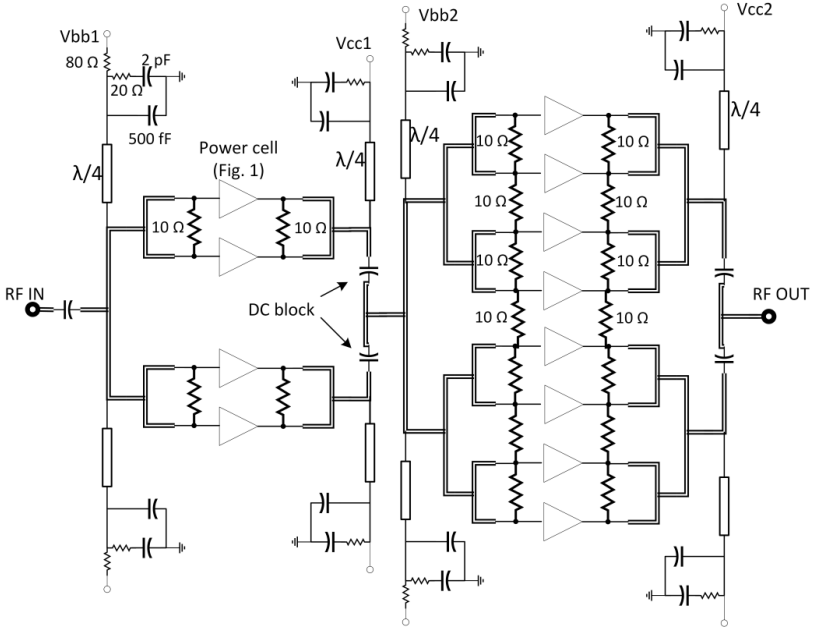
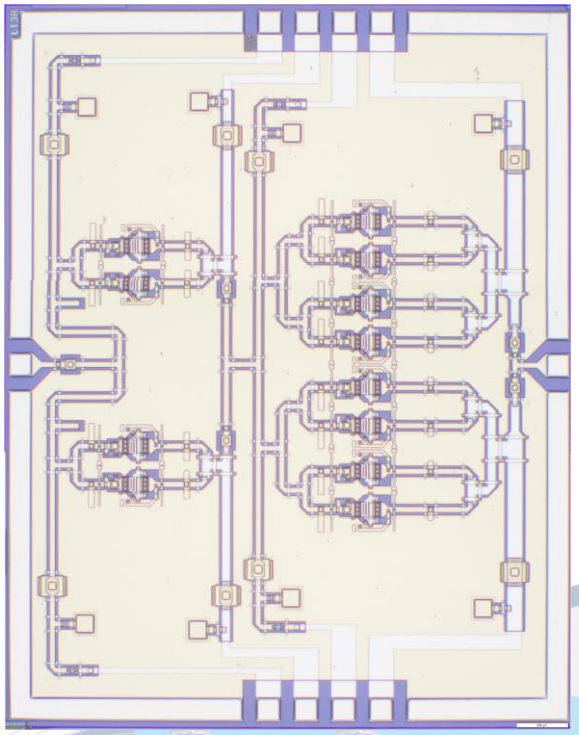
Two-stage 8-way power amplifier





2.4 × 3 mm²

Bias settings

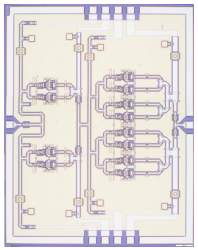
Vbb1=1.7 V
Ibb1=4,1 mA

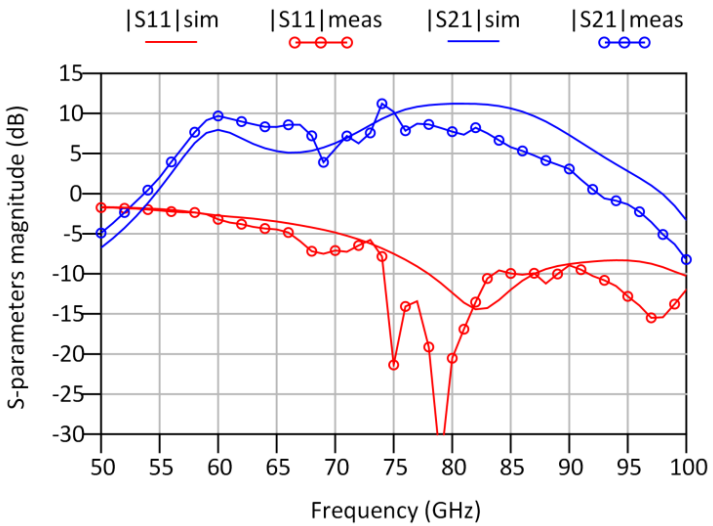
Vcc1=4 V
Icc1=172 mA

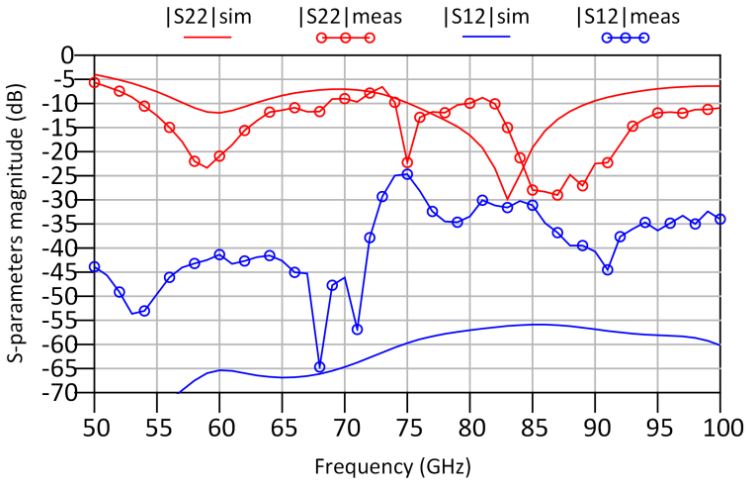
Vbb1=2 V
Ibb1=8 mA

Vcc2=4,5 V
Icc2=340 mA

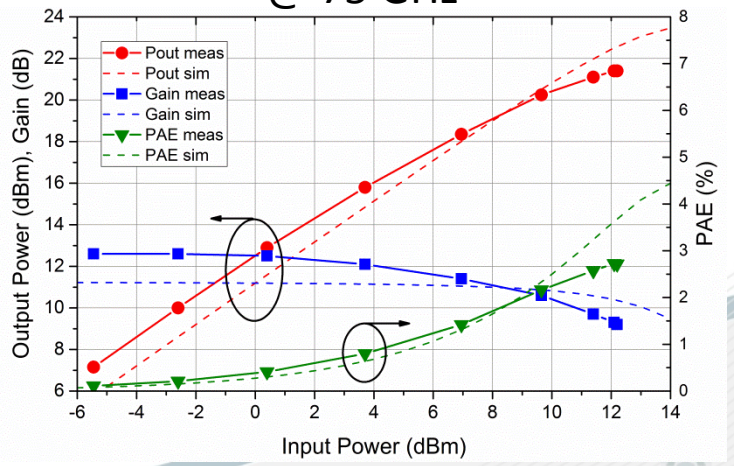
Two-stage 8-way power amplifier







@ 75 GHz



- Gain ≈ 12 dB
- $P_{out,1dB}$ ≈ 18 dBm
- P_{sat} > 21 dBm

Microwaves for the Internet of Things

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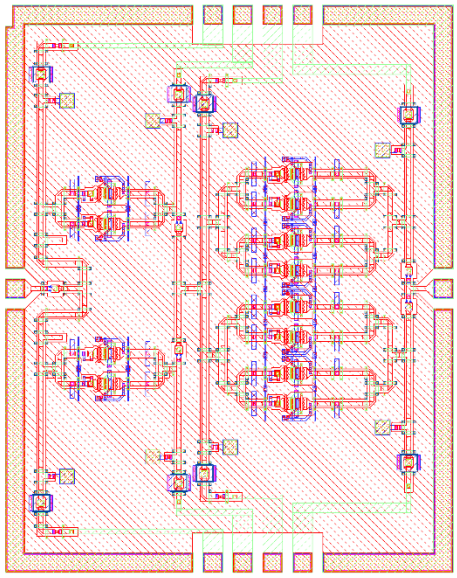
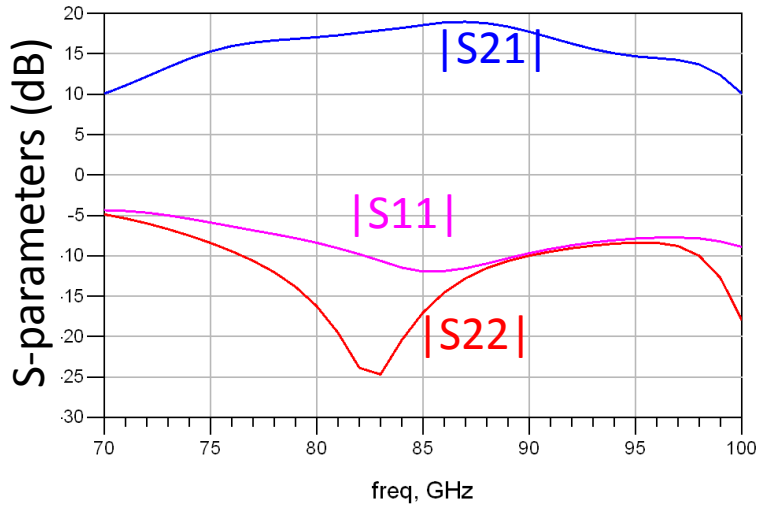
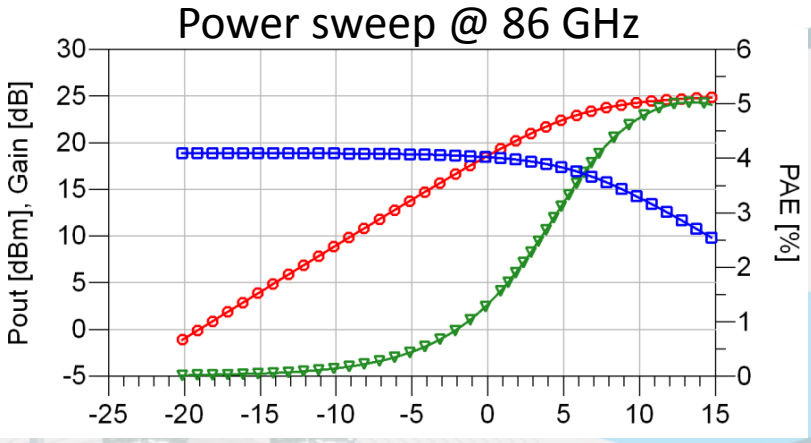
Ongoing and future works

Simulation results on power optimized process SAND



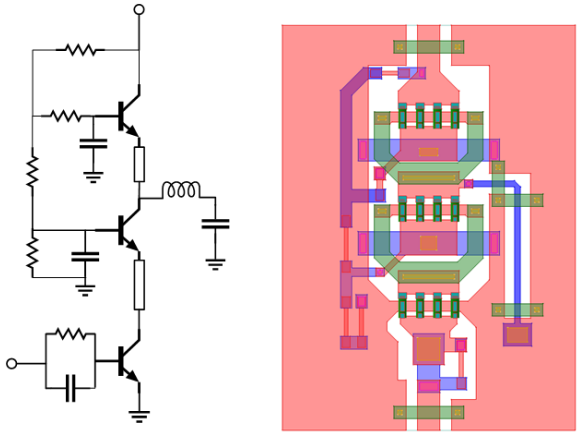
- Gain ≈ 18 dB
- $P_{out,1dB}$ ≈ 22 dBm
- P_{sat} > 24 dBm



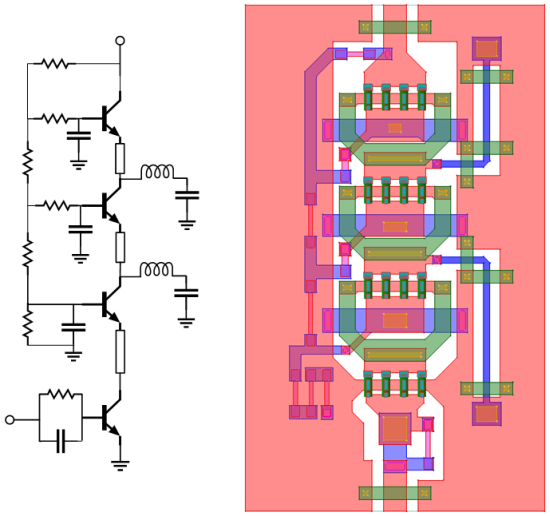


Ongoing and future works

Three-stacked transistor

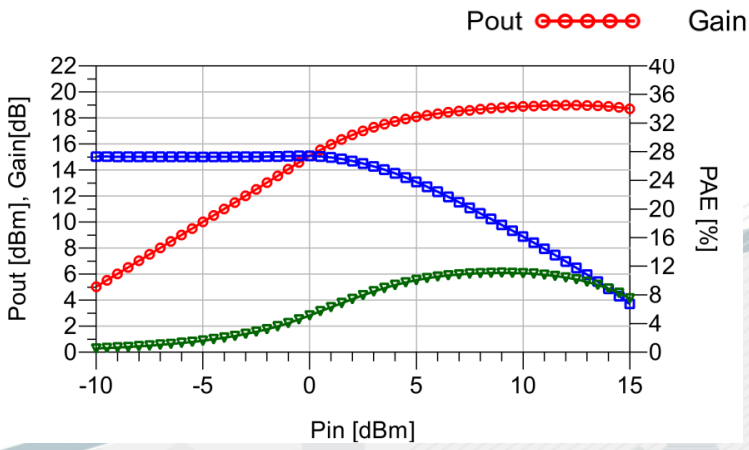


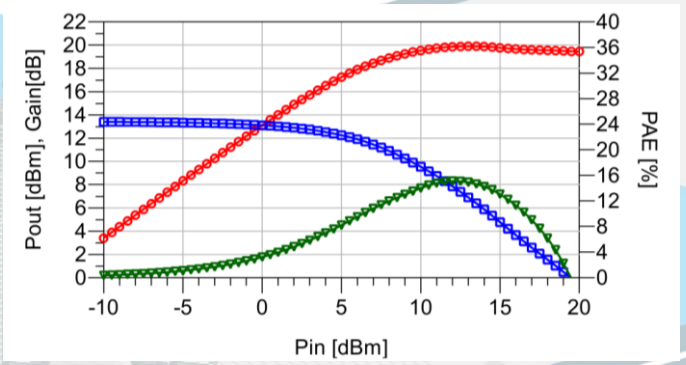
Four-stacked transistor



Preliminary results (SAND process)

Simulated power sweep at 86 GHz





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Summary and conclusions

- This work represents an attempt to extend the stacked-transistor concept to InP DHBT technology in order to get higher performances in terms of output power, gain and efficiency.

- A two-stage eight-way 75 GHz power amplifier based on two-stacked transistors has been designed and tested.
  $G \approx 12$ dB, $P_{out,1dB} \approx 18$ dBm and $P_{sat} > 21$ dBm have been obtained experimentally.

- Better performances are expected from a power optimized process currently under development.

- Three- and four-stacked power cells under investigation with promising preliminary results.

Acknowledgments

III-V lab

European Commission

IN-POWER

SEVENTH FRAMEWORK PROGRAMME

InP DHBT MMIC Technology for Millimeter-Wave Power Applications

Microwaves for the Internet of Things

Acknowledgments

Thank you for your attention!