Design Procedure for Millimeter-wave InP DHBT Stacked Power Amplifiers

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Abstract — The stacked-transistor concept for power amplifiers (PA) has been investigated in this work. Specifically, this architecture has been applied in the design of millimeter-wave monolithic microwave integrated circuits (MMICs) using indium phosphide (InP) double heterojunction bipolar transistors (DHBTs). In this paper we describe the design methodology adopted and the results obtained at 86 GHz and 140 GHz. In the former case, 14.5 dBm of output power at the compression point, 14.5 dB of gain and 19.6 % of PAE are obtained from a four-transistor power cell. At 140 GHz, the same architecture gives 13.1 dBm of output power, 10.1 dB of gain and 13 % of PAE. To the best of the authors' knowledge, this is the first investigation of multi-level stacked PAs based on InP HBT technology.

Index Terms — Heterojunction bipolar transistor (HBT), Millimeter wave integrated circuits, MMIC, power amplifier, stacked transistors.

I. Introduction

Recently, wireless communications and radar applications are increasingly taking place at millimeter-wave bands. The aim behind this trend is to exploit the large bandwidths available at these frequencies. It is well known, however, that the main limitations of these systems are imposed by the power amplifier capabilities. In MMIC technology, one of the most challenging issues is the limited breakdown voltage of the transistors, which limits the output voltage swing. This aspect is becoming more and more critical with the continuous downscaling of devices.

To overcome the limited breakdown voltage, the series combination of transistors in stacked architectures is currently under investigation [1]-[4]. Stacking *n* devices, the overall output voltage swing can be *n* times larger than a single device and, as the current swing is the same, it results in an output power *n* times higher. Moreover, the optimum load impedance is increased by the same factor *n*, allowing the implementation of low-loss and broadband matching networks. In order to optimize the output power, the voltages across the devices must be of the same amplitude and phase-aligned. The latter condition is particularly challenging at millimeter-wave frequencies due to parasitic effects. This stacking concept has been widely investigated with FET transistors, but only a few works have been applied to bipolar transistors (e.g. [5]).

InP DHBT technology has proven attractive for its power handling capabilities at high millimeter-wave frequencies [6]. A millimeter-wave interstage matched Cascode configuration in InP DHBT was reported in [7]. In this work we investigate the possibility to implement multi-level stacked power amplifiers by using InP DHBTs at high millimeter-wave frequencies. We describe the procedure that can be followed in the design-flow of a stacked power-cell. This methodology has been adopted at two different frequencies (86 GHz and 140 GHz) and the corresponding results are compared.

II. Devices And Circuit Overview

In this work, InP DHBT single-finger devices are used to investigate the circuit topology. They are characterized by a collector-emitter breakdown voltage BV_{CE0}=4.9 V and f_T/f_{max}=330/420 GHz when biased at Vce=2.4 V and I_C=15 mA. In the design process, the non-linear UCSD HBT model is employed in circuit simulations.

In Fig. 1, the architecture of a four-transistor stacked power cell is shown. At the output of the common-emitter stage, a series of common-base stages is connected. The base terminals are connected to finite impedances through the capacitances C_k, so they are not tied to the ground voltage. This reduces the base-collector voltage swing and the relative breakdown is prevented. In order to maximize the performances of the circuit, each transistor should be matched

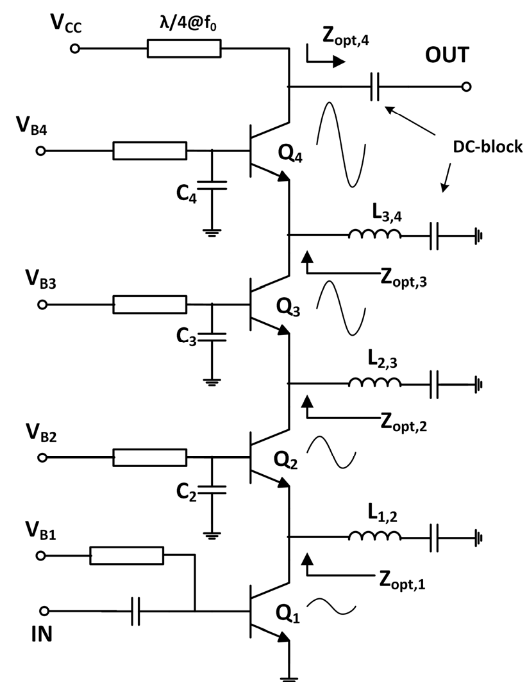

Fig. 1. Circuit schematic of a four-transistor stacked power cell.

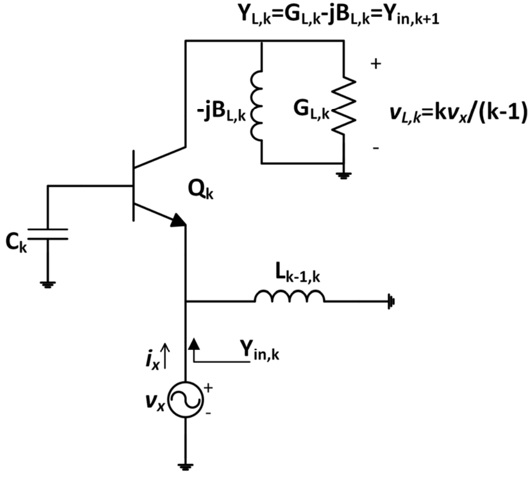

Fig. 2. Circuit schematic of the k-th stage of the power cell used to estimate C_k and $L_{k-1,k}$ (bias details omitted).

for maximum output power, and the corresponding optimum impedance $Z_{opt,k}$ should be connected to its output. For this purpose, shunt inductors $L_{k-1,k}$ are used as inter-stage matching between the transistors.

The amplitude of the overall output voltage is equally distributed among the devices. Moreover, for efficient power combining and for preventing collector-emitter breakdown, voltage phase-alignment is required. The following expression has to be satisfied:

$$v_{c,k} = \frac{k \cdot v_{c,k-1}}{k-1}, \tag{1}$$

$v_{c,k}$ being the collector voltage of the k-th transistor.

All these requirements are accomplished by properly choosing the values of C_k and $L_{k-1,k}$ as described next.

III. Design Methodology

The first step in the design of the stacked power cell is to identify the optimum load of the common emitter-stage ($Z_{opt,1}$) through a load-pull simulation. The input impedance to the second stage, then, should be identical. In this regard, the circuit of Fig. 2 is used to evaluate $Y_{in,2}$, which is directly related to the values of C_2, $L_{1,2}$, and to the load admittance $Y_{L,2}$, which will coincide with the input admittance of the third stage. Due to the parasitic capacitances of the transistor, it is expected that the load susceptance must be negative.

In order to comply with (1), the first guess of the design is done by setting $G_{L,2} = 0.5 \times \mathrm{Re}\{1/Z_{opt,1}\}$. In this condition, the values of C_2 and $B_{L,2}$ must be found in such a way to make v_x and $v_{L,2}$ phase-aligned and $\mathrm{Re}\{Y_{in,2}\}=\mathrm{Re}\{1/Z_{opt,1}\}$. At this point, v_x and $v_{L,2}$ are close to satisfy (1), but not exactly. In fact $v_{L,2} < 2 \cdot v_x$ due to the intrinsic ohmic losses of the transistor that are taken into account in the model. For this reason, $G_{L,2}$ is slightly decreased and a new iteration is carried out. This procedure can be repeated a few times until

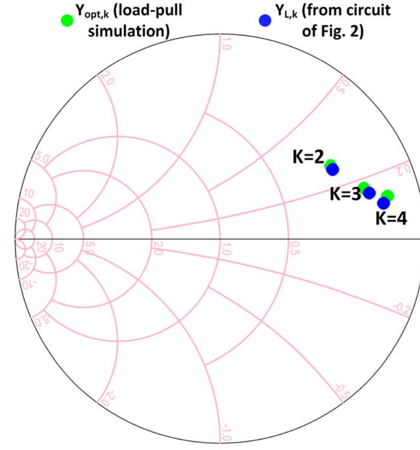

Fig. 3. Comparison between the admittances found by load-pull simulations (green) and the ones previously found (blue).

(1) is perfectly satisfied. The next step is to make $\mathrm{Im}\{Y_{in,2}\}=\mathrm{Im}\{1/Z_{opt,1}\}$ by properly tuning the value of $L_{1,2}$. At this point, a two-transistor power cell has been designed. If we perform a load-pull simulation on this power cell, it turns out that the optimum load admittance $1/Z_{opt,2}$ is close to $Y_{L,2}=G_{L,2}$-$jB_{L,2}$ just found, so the latter could be used as the starting point to design the third stage following the procedure just described.

In the Smith chart of Fig. 3, the optimum load admittances found in load-pull simulations for each stage are reported together with the admittances $Y_{L,k}$ found following our methodology. In some sense, their proximity is not surprising, as an admittance found from load-pull different from $Y_{L,k}$ would cause a mismatch between Q_k and Q_{k+1}, and hence a loss of power.

IV. Simulation Results

Following the design-flow described above, two four-transistor power cells have been implemented: one at 86 GHz

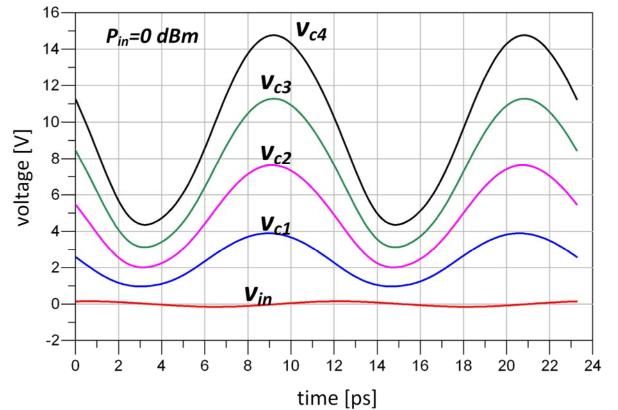

Fig. 4. Simulated voltage waveforms at each collector of the four-transistor stacked power cell at 86 GHz

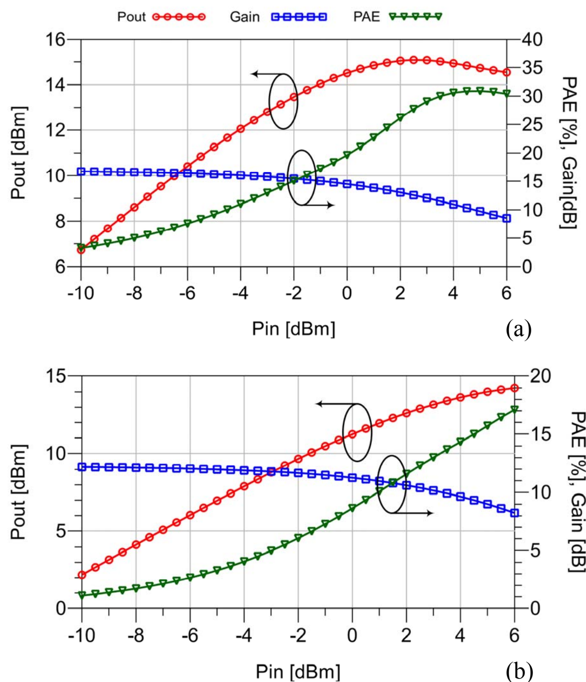

Fig. 5. Power sweep simulation of the four-transistor stacked power cells at 86 GHz (a) and at 140 GHz (b)

and one at 140 GHz, respectively. In Fig. 4, the voltage waveforms at each collector are depicted together with the input voltage waveform at 86 GHz. The input power has been set to P_{in}=0 dBm, which corresponds to the 1-dB compression point of the power cell designed at 86 GHz. It can be seen that the breakdown voltage of 4.9 V is never exceeded and (1) is satisfied in magnitude as well as in phase. This guarantees a high efficiency of the stacked power cell. A similar set of waveforms is obtained for the 140 GHz power cell and also in this case the condition (1) is satisfied.

Power sweep simulations have been carried out on the two power cells and the relative results are compared in Fig. 5. At the compression point, the power cell designed at 86 GHz exhibits an output power of 14.5 dBm, a gain of 14.5 dB and a power-added efficiency (PAE) of 19.6 %. For the power cell designed at 140 GHz, compression occurs with an input power equal to 3 dBm. At this point the output power is 13.1 dBm and the corresponding gain is 10.1 dB and PAE is 13 %.

It is clear that during the design flow of the four-transistor power cell, the intermediate steps are the design of the two- and three-transistor power cells. The output power of them has been monitored as well. In Fig. 6, the output power as a function of the number of transistors has been reported for both cases (86 GHz and 140 GHz). Taking the common-emitter stage as a reference (one-transistor), it can be seen that the total incremental output power is 5 dBm for the 86 GHz case and 4.5 dBm for the 140 GHz case.

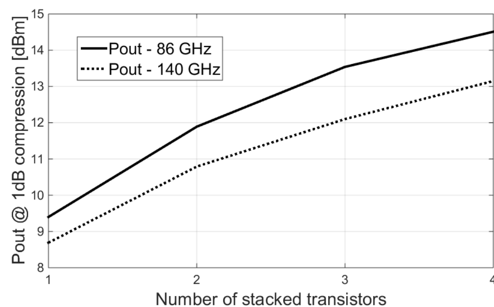

Fig. 6. Output power as a function of the number of stacked transistors

V. Conclusions

In this work we have investigated the possibility to apply the transistor-stacking concept to InP DHBT power amplifiers operating at high millimeter-wave frequencies. An effective design procedure has been described and applied to two different four-transistor stacked power cells operating at 86 GHz and 140 GHz, respectively. As expected, the performance is better at 86 GHz, however, the output power at 140 GHz is comparable and a driver amplifier could be used for compensating the lower gain. This work can pave the way for new millimeter-wave stacked power amplifier topologies still unexplored in InP technology.

VI. Acknowledgement

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