Design of a Planar Ultra-Wideband Four-Way Power Divider/Combiner Using Defected Ground Structures

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***Abstract*—This work presents the design of a planar ultra-wideband (UWB) four-way power divider/combiner. A prototype has been fabricated on a printed circuit board and characterized. For achieving the frequency response required in UWB applications, each branch of the divider is conceived as a three-section Chebyshev impedance transformer. The defected ground structure (DGS) technique has been used to obtain the required high impedance lines. The power divider's insertion loss is 1 dB at 3.1 GHz and 2.9 dB at 10 GHz; the input reflection is lower than -10 dB, and the isolation between the output ports is better than 13 dB from 3 GHz to 10 GHz. A back-to-back configuration has been implemented as well. Its insertion loss is lower than 5 dB and its input reflection is lower than -10 dB over the UWB frequency range.**

***Keywords*—Power divider; ultra-wideband; defected ground structure.**

I. Introduction

Equiphase and equiamplitude *n*-way power combiners/dividers are essential components in many microwave systems, including power amplifiers, oscillators and antenna arrays. The Wilkinson power divider is perhaps the most popular due to its simple design and good performances in terms of losses, matching and isolation [1]. In the original formulation, the Wilkinson power divider utilizes a single quarter-wavelength impedance transformer section, which limits its fractional bandwidth. A wider bandwidth can be attained by means of a multiple-section divider, where each line is a stepped-impedance transformer designed for a maximally flat or equiripple response [2], [3]. The working principle, in either case (single- or multiple-section), relies on the electrical symmetry of the structure, allowing the isolation resistors to be connected to a central common node and suppress odd-mode propagations. For a planar implementation, known as fork power divider, perfect electrical symmetry is harder to obtain (unless *n*=2), and compensation techniques have to be adopted to make the external lines having the same electrical characteristics as the internal ones [4]. The corporate power combiner/divider, employing several 2-way Wilkinson, can offer an increased level of symmetry [5]-[7], but it is limited to cases where *n* is a power of two. Moreover, it may occupy a large area and exhibit relatively high losses [8], [9].

In this work, the design of a planar four-way three-section power combiner/divider suitable for ultra-wideband (UWB) applications is presented [10]. It provides a frequency range spanning from 3.1 GHz to 10.6 GHz and features a Chebyshev response. In such a design, lines with a high characteristic impedance are needed. Given a microstrip technology with a fixed substrate, the way to increase the characteristic impedance is to reduce the line width, eventually down to the limit of reliable manufacturability. To overcome this limit and obtain even higher values, the Defected Ground Structure (DGS) technique [11] has been exploited in this design. By lengthening the return path of the current, a higher value of the series inductance is obtained, so a line with high characteristic impedance has been realized and used as the first section of the Chebyshev power divider

In what follows, the circuit description and the design procedure of the divider are summarized. Its implementation and experimental results are reported. A back-to-back configuration is also presented with measurements results.

II. Circuit Design

A general schematic diagram of a three-section four-way power divider is shown in Fig. 1. A rigorous analysis should consider all possible excitation modes (one even-mode and three odd-modes in this case) and, by imposing a specific response in terms of reflection coefficients and isolation, should provide design formulas for calculating the characteristic impedances Z_k and the isolation resistances R_{kx} and R_{ki} (k=1,2,3) [12]. θ_k denotes the electrical length of the

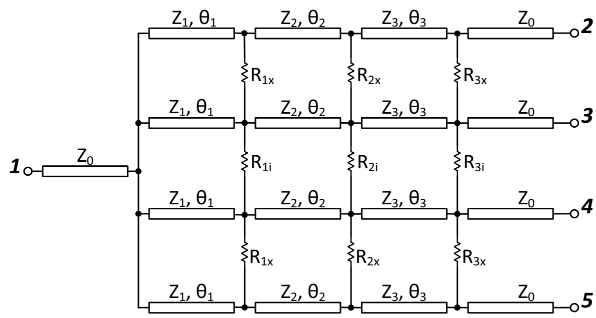


Fig. 1. Circuit schematic of a planar three-section four-way power combiner/divider

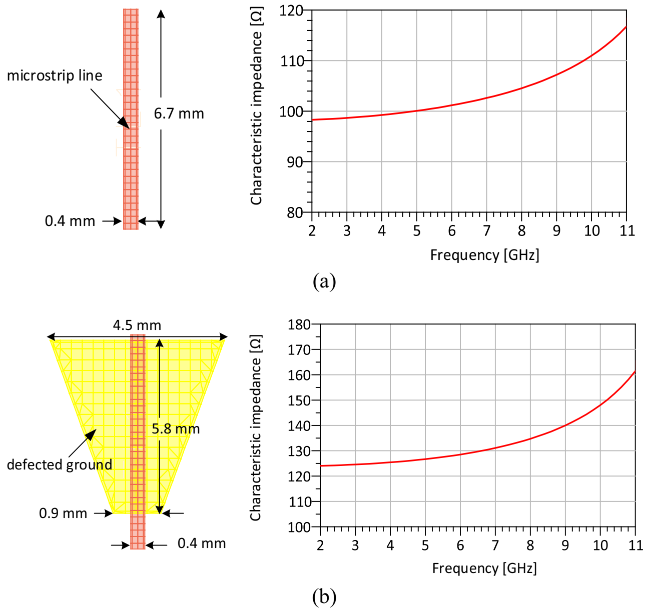


Fig. 2. EM-simulated characteristic impedance for a standard microstrip line (a) and for a microstrip with DGS structure (b) on Rogers RO4003C.

lines and should be equal to π/2 at the center frequency (7 GHz in our case). The design starts by considering the even-mode equivalent circuit, which consists of a three-section stepped-impedance line with characteristic impedances Z_k, transforming the Z_0 load up to $4Z_0$. In this design, it was decided to optimize the bandwidth and tolerate a small ripple, so the choice was to make the reflection coefficient having a Chebyshev response with a maximum value of -10 dB over the UWB frequency range. Considering the standard load termination Z_0=50 Ω and referring to the well-known tables available in the literature [2] led us to select Z_1=140 Ω, Z_2=100 Ω and Z_3=70 Ω. Isolation resistors can be found by imposing the suppression of all odd-modes. Exact theoretical formulas are given in [12] and in this case they give $R_{1x}=R_{1i}$=44 Ω, $R_{2x}=R_{2i}$=152 Ω and $R_{3x}=R_{3i}$=300 Ω. Because of the not perfect electrical symmetry, in real design $R_{kx}\neq R_{ki}$ resulted, and slightly different values were obtained after EM optimization. Moreover, the connections between the resistors introduce significant parasitic effects that harm the performances of the divider [13], and they have been taken into account and alleviated as much as possible.

III. Microstrip Implementation

A. Technology

The technology selected for this power divider is Rogers RO4003C, a 0.81 mm thick ceramic substrate with relative permittivity ε_r=3.55 and tanδ=0.0022 at 10 GHz, 35 µm thin copper layers on top and bottom. Resistors are implemented with S0402 SMD components. Keysight ADS has been used for circuit and EM simulations.

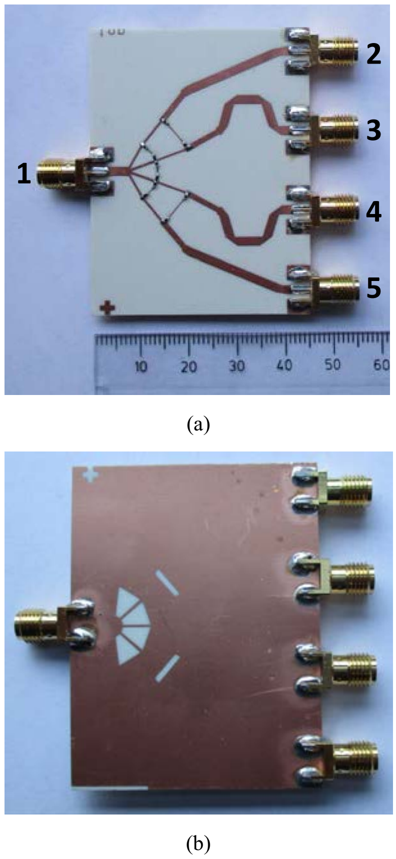


Fig. 3. Top (a) and bottom (b) views of the fabricated power divider/combiner

B. Defected Ground Structures

With the available fabrication tools, an acceptable accuracy is guaranteed for lines wider than 0.4 mm. In Fig. 2a, the layout of a 6.7 mm long (corresponding to a quarter-wavelength), 0.4 mm wide microstrip line is shown with its characteristic impedance obtained from EM simulations. In this technology, around 100 Ω has been obtained over the UWB frequency range, so it works for the second section of the impedance transformer. To obtain Z_1=140 Ω, a DGS has been drawn underneath a line of the same width (Fig. 2b). In light of the radial configuration of the full power divider, where all lines converge to the common input port, a trapezoidal shape has been selected for the DGS structure, whose dimensions have been established after an iterative optimization process. EM simulation results show a significant increase of the characteristic impedance. The DGS technique proved to be beneficial also when applied to the resistors' connections. Indeed, by lowering their parasitic capacitance to ground, it allows the frequency response of the divider to be unaffected.

C. *Power Divider Layout*

In Fig. 3a and 3b, the top view and the bottom view of the power divider are illustrated, respectively. Excluding the SMA connectors, it has a 44.9×57.8 mm^2 area. Having all output ports geometrically aligned, it is well suited for power amplifier applications, where it can be used as a combiner as well. A high combining efficiency is ensured by bending the central lines so that all ports have the same phase characteristics. EM simulations in ADS Momentum and iterative optimizations allowed us to select the optimum line widths and resistors' values, summarized in Table I. It was found that resistors R_{2i}, R_{3i} and R_{3x} do not improve isolation and matching significantly. Instead they introduce extra-losses, so they were eliminated from the design.

TABLE I. OPTIMIZED LINE WIDTHS AND RESISTOR VALUES

	k=1	*k=2*	*k=3*
Z_k	0.4 mm with DGS (140 Ω)	0.4 mm (100 Ω)	1.1 mm (70 Ω)
R_{kx}	86.6 Ω	340 Ω	*open*
R_{ki}	316 Ω	*open*	*open*

IV. MEASUREMENTS RESULTS AND DISCUSSION

Measurements have been carried out using the two-port VNA Hewlett Packard 8720D and compared with EM simulation results. In Fig. 4a, the insertion loss and the input reflection of the divider are reported. The reflection is well below -10 dB from 2.5 GHz to 11 GHz, even outperforming the UWB requirements, and it has the desired typical shape of a third order Chebyshev polynomial. In addition to the theoretical 6 dB, the insertion loss of the four-way power divider is 1 dB at 3.1 GHz and slightly increases at higher frequencies, reaching 2.9 dB at 10 GHz. Rather than being a design-related issue, it can be easily attributed to the relatively low-cost technology. Indeed, good agreement can be seen between simulations and measurements. In Fig. 4b, the output ports reflections are shown. Due to the adopted tradeoff between losses and matching in selecting the resistors, the output matching is not perfect, especially below 4 GHz, where the divider exhibits up to -6.5 dB of reflection at 3.1 GHz. At higher frequencies it behaves better, and only in a few frequency points the reflection is higher than -10 dB. Another issue that can be noted from these plots is the relative asymmetry: while internal ports 3 and 4 are practically identical, a small difference exists between the external ports 2 and 5. Again, this is due to fabrication uncertainties rather than design issues. Isolation between the output ports is reported in Fig. 4c. The best isolation performances are seen between ports 3 and 4, being better than 15 dB over the whole UWB range. Only slightly worse, 14 dB, is the isolation between ports 2 and 4. In all other cases, 13 dB, at worst, is observed.

The electrical symmetry of the proposed power divider can be further analyzed by looking at Fig. 5a and Fig. 5b, where the measured amplitude imbalance and phase imbalance are reported, respectively, and compared with simulations. The highest amplitude imbalance exhibited by the power divider is 0.6 dB in absolute value. Performance degradation is more significant only above 7 GHz. While the amplitude imbalance between ports 2 and 3 can be attributed to the different electrical characteristics between the lines (straight and bended for instance), the imbalance between ports 2 and 5, which should be perfectly symmetric, can only be due to fabrication and/or resistors' uncertainties. Regarding the phase imbalance reported in Fig. 5b, it can be seen that it is only 4º under 8 GHz between all ports. At higher frequencies, the phase imbalance reaches 6º between ports 2 and 4, and 8º between ports 2 and 5.

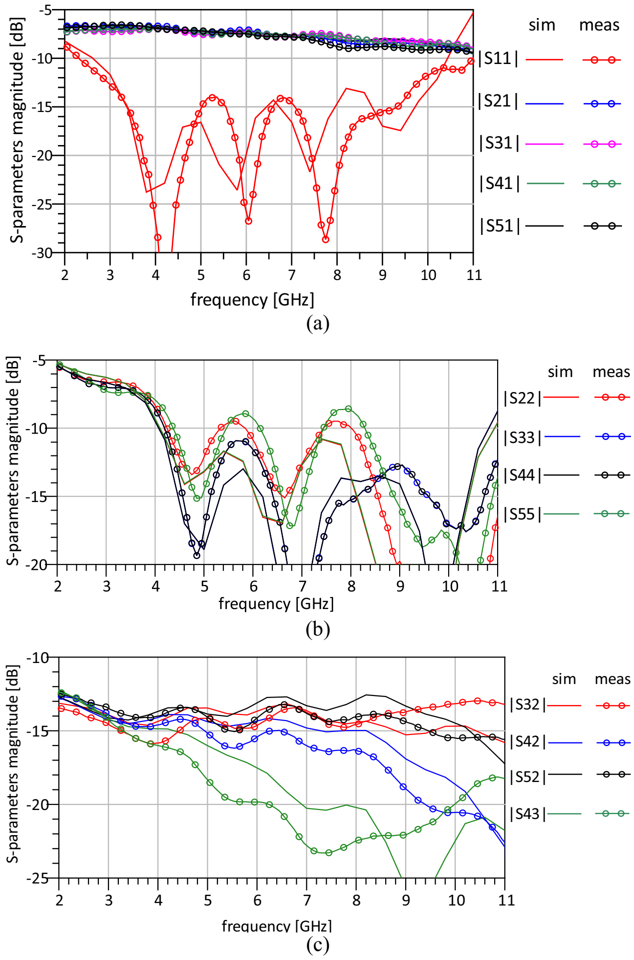
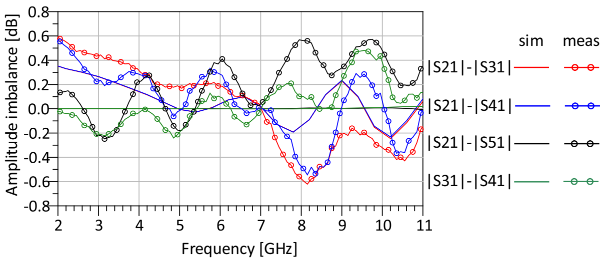
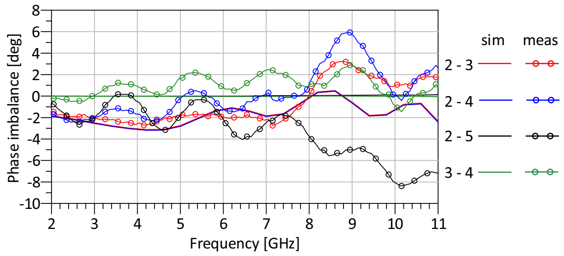


Fig. 4. Simulated and measured responses of the power divider: input reflection and insertion loss (a); ouput reflections (b); isolation between the output ports (c).



(a)



(b)

Fig. 5. Simulated and measured amplitude imbalance (a) and phase imbalance (b) of the power divider.

V. Back-to-Back Configuration

In power amplifier design, it is common practice to employ several power devices in parallel in order to achieve higher RF transmitting power, so a power divider is needed to split the input signal. Unless the amplified signals are fed to a transmitting antenna array, they need to be recombined. This is often done by reversing a copy of the divider. To account of all the losses taking place in the passive circuits of the power amplifier, the performances of a back-to-back structure have been investigated. In Fig. 6a, the back-to-back configuration of our power divider/combiner is shown, and in Fig. 6b, its measured frequency response is reported and compared with simulations. Besides the good agreement between the two, it can be seen that the insertion loss is lower than 2 dB at 3 GHz, but increases at higher frequencies, reaching 5 dB at 10 GHz. Reflections are lower than -10 dB.

VI. Conclusions

In this work, an ultra-wideband planar four-way power divider/combiner with a Chebyshev response, suitable for power amplifiers, has been designed and investigated. The defected ground structure technique has been used to realize the high impedance lines. Some tradeoffs in the choice of the isolation resistors and a relatively low-cost technology are responsible for moderate losses at high frequencies. Very good agreement between measurements and simulations has been observed. Prospective works could include implementations of the same concept on other technologies and/or higher frequencies of operation, eventually millimeter-waves.

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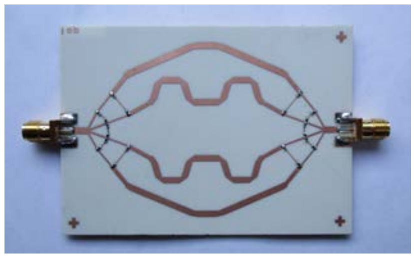
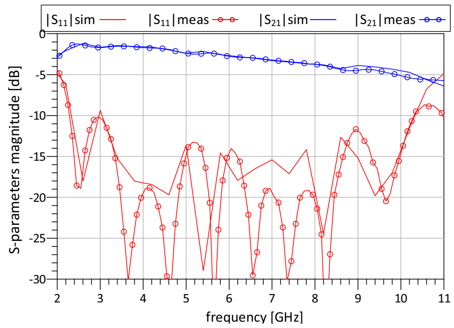


(a)



(b)

Fig. 6. Back-to-back power divider top view (a) and S-parameters (b).

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