InP DHBT MMIC Power Amplifiers for mm-Wave Applications (IN-POWER)

PhD student:

Michele Squartecchia

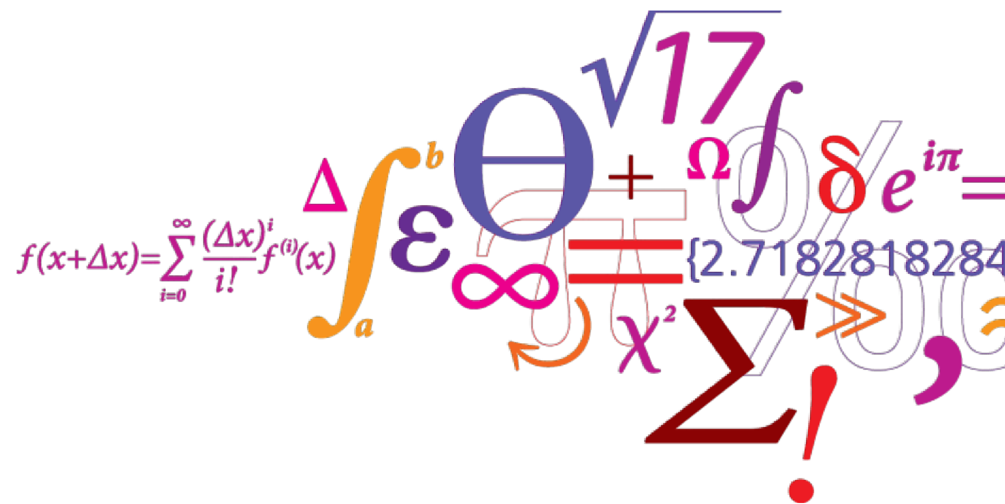
Supervisors:

Tom K. Johansen (DTU)

Jean-Yves Dupuy (III-V Lab)

Company partner:

III-V Lab (Paris, France)



DTU Electrical Engineering

Department of Electrical Engineering

Outline

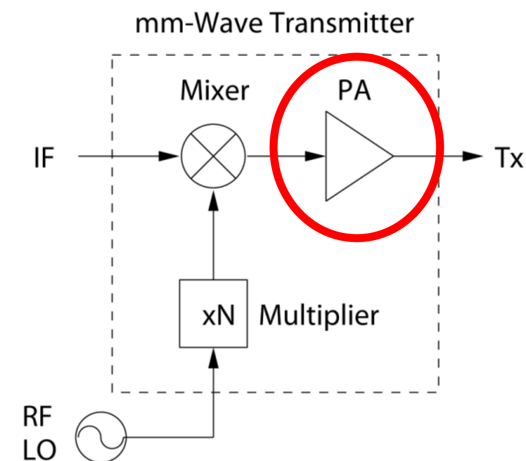
- Background and Motivation
- Power cell design
  - Procedure
  - Preliminary results
- Ongoing work
- Future Work

Background and Motivation

- Due to the needs for high-speed data transmission, wireless communications are increasingly taking place at E-band (71-76 GHz, 81-86 GHz) and higher millimeter-wave bands
  - Large absolute bandwidth
  - Low atmospheric attenuation
  - Small system size
  - Highly directive antennas

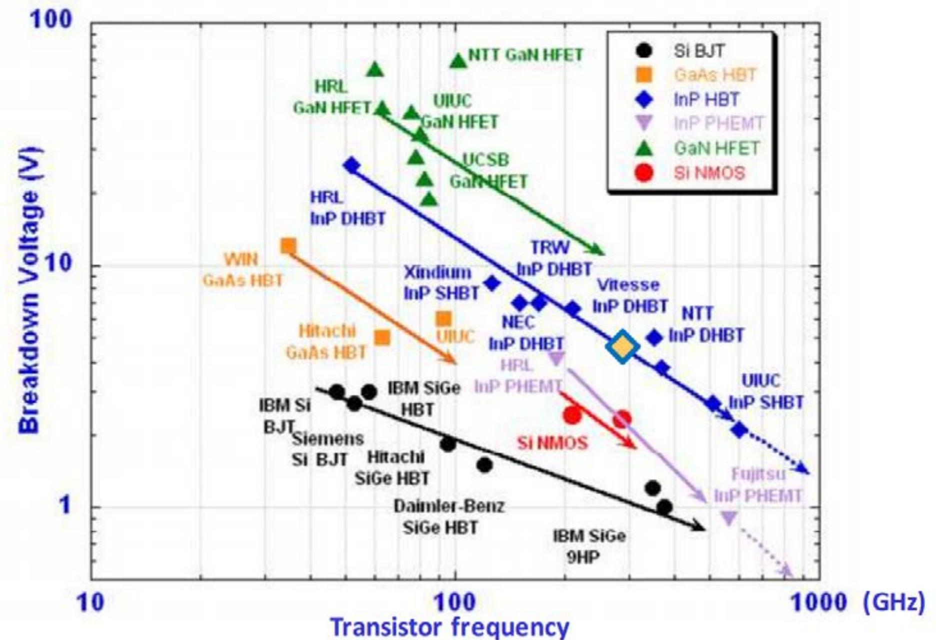
- At mm-waves, the main limitations are imposed by the power amplifier of the transmitter ($P_{Tx} \sim 1/f^2$)

- Geometrical downscaling of devices leads to high operation frequencies, but also to limited breakdown voltages



Background and Motivation

- Compared with other semiconductors, InP Double Heterojunction Bipolar Transistor (DHBT) technology offers a combination of very high frequency of operation and high voltage signal swing together with the potential for high density of integration

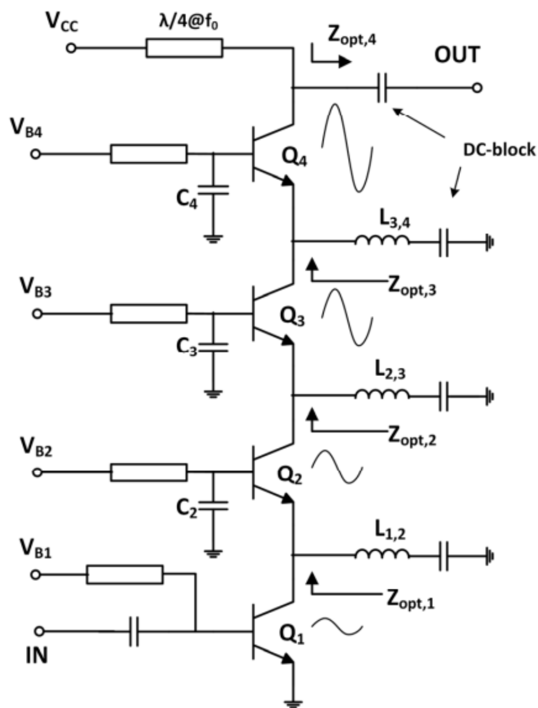


Objective

- Investigation and design of innovative circuit topologies to maximize transmitted power and efficiency, minimizing signal distorsions

Power cell design

- InP DHBTs have a good breakdown voltage, but still limited...
- Series combination of transistors in stacked architecture



- Stacking *n* devices, the overall output voltage swing can be *n* times larger than a single device
- The current swing remains the same
- The optimum load impedance is increased by the same factor *n*

⇨ <u>Output power *n* times higher</u>

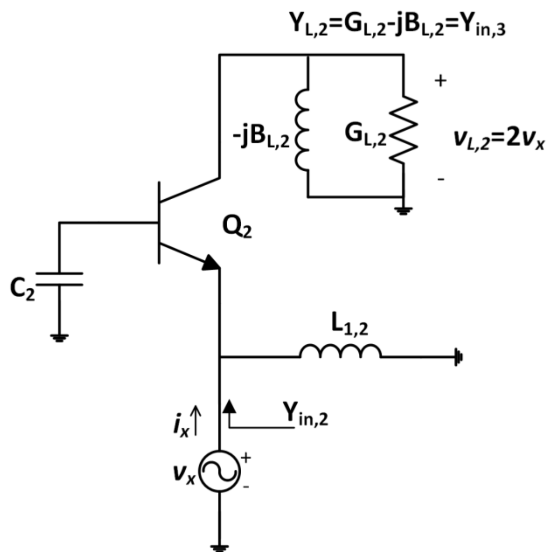
- For efficient power combining and for preventing collector-emitter breakdown, the overall voltage swing is equally distributed, and phase-alignment is required:

$$v_{c,k} = \frac{k \cdot v_{c,k-1}}{k-1}$$

Power cell design

Procedure:

- Load pull simulation for the common-emitter stage ($Z_{opt,1}$)
- The input impedance to the second stage should have the same value



- $1/G_{L,2}=2\times\mathrm{Re}\{Z_{opt,1}\}$
- $B_{L,2}$ and C_2 for phase alignment and $\mathrm{Re}\{Y_{in,2}\}=\mathrm{Re}\{Z_{opt,1}\}$
- $L_{1,2} \longrightarrow \mathrm{Im}\{Y_{in,2}\}=\mathrm{Im}\{Z_{opt,1}\}$

- It can be shown that the value of $Y_{L,2}$ found in this way coincides with the optimum value that would be found through load-pull simulation performed on the resulting two-stack power cell

- The same procedure can be carried out for the design of the third and fourth stages

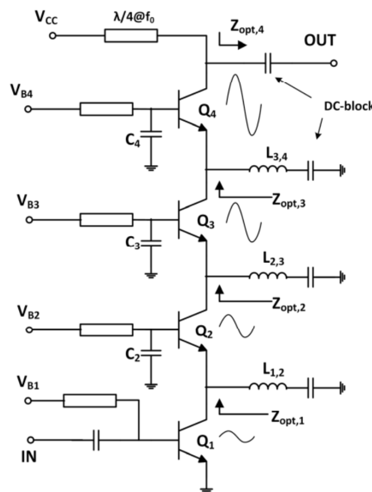
Power cell design

Preliminary results:

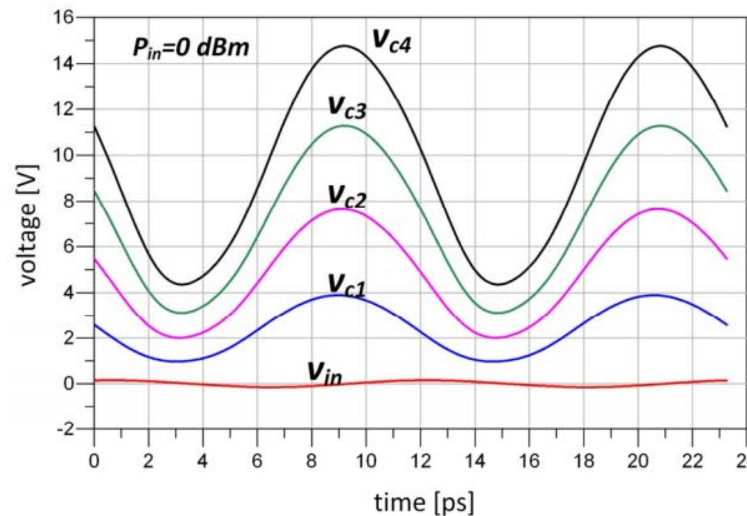
- InP DHBT single finger devices

  BV_{CE0}=4.9 V; f_T/f_{max}=330/420 GHz @ V_{ce}=2.4 V and I_c=15 mA

- The non-linear UCSD HBT model is employed for circuit simulations



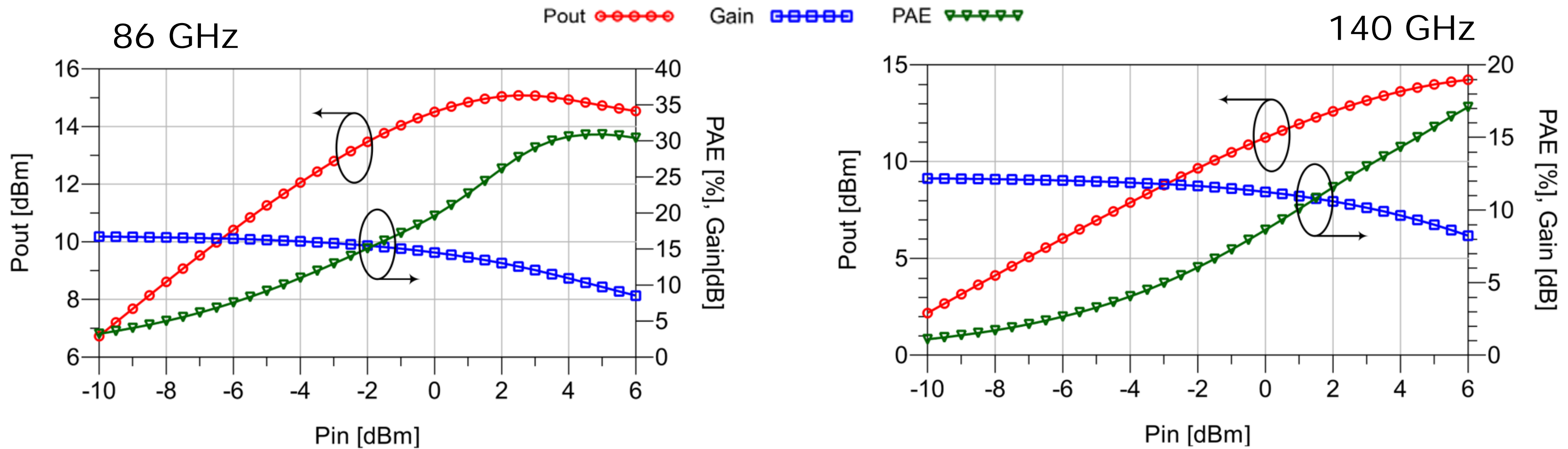
Collector waveforms at the 1-dB compression point



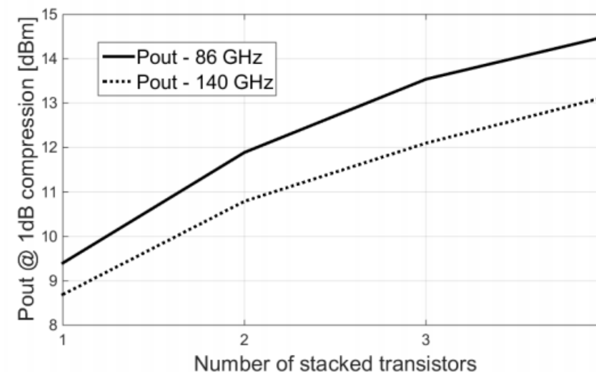
@ 86 GHz

Power cell design

Preliminary results:

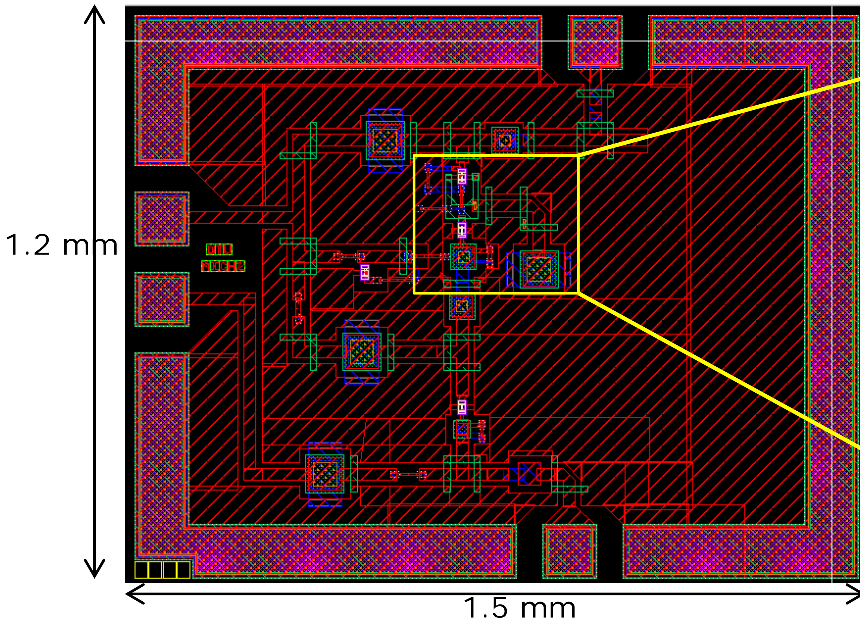


The design of the two- and three-stack power cells are intermediate steps for the design of the four-stack

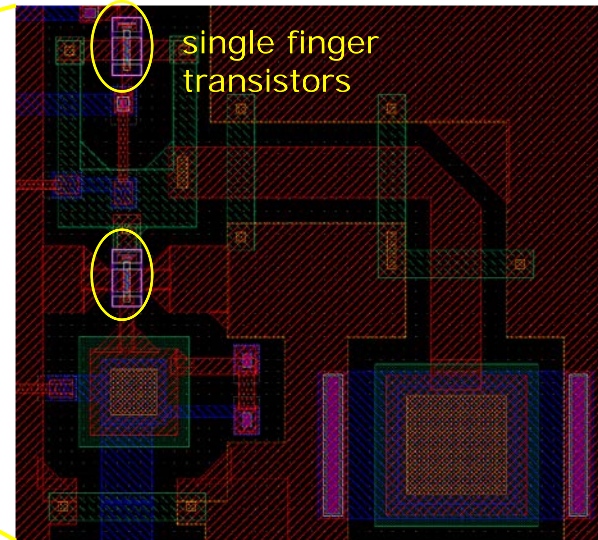


Power cell design

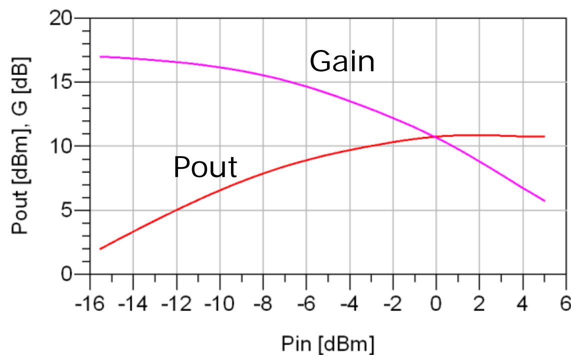
Preliminary results:

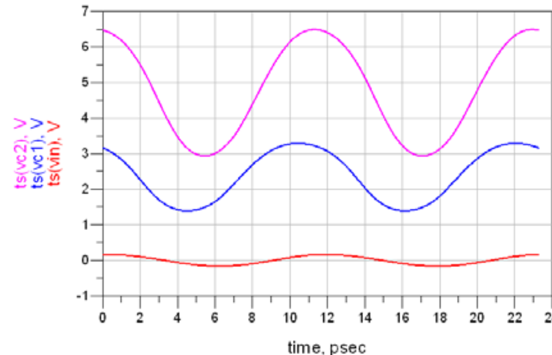


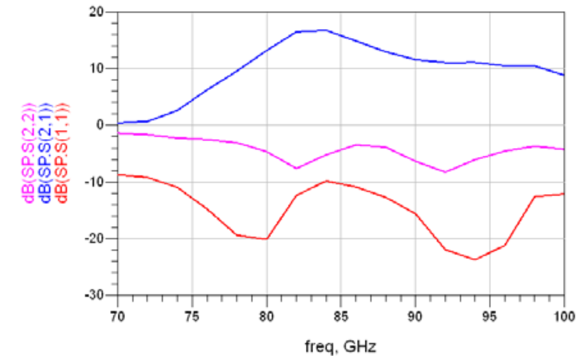
Power cell



Electromagnetic simulations

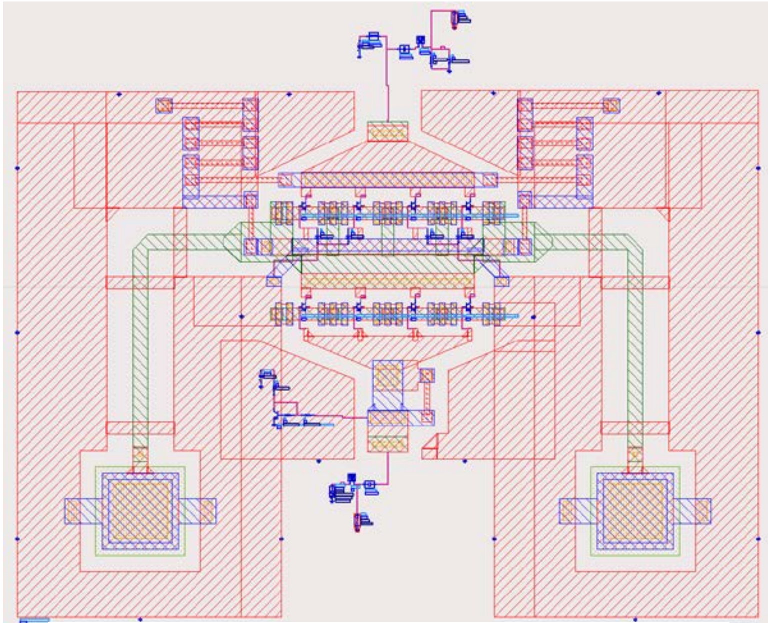




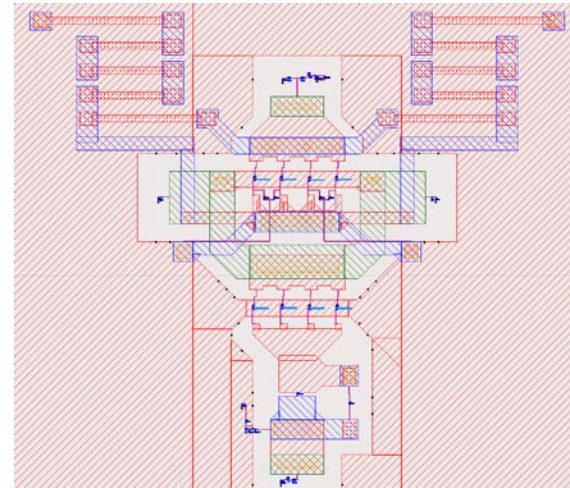


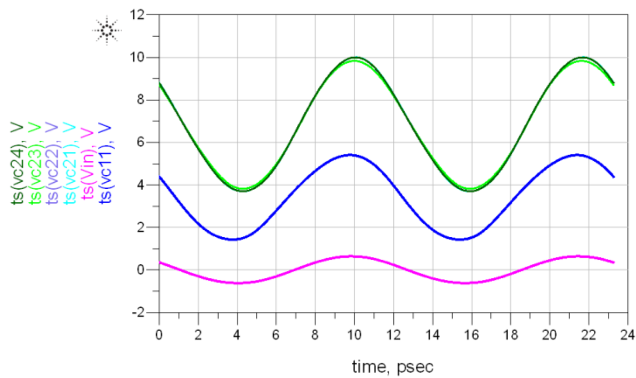
Ongoing work

two-stack 4-finger ballasted transistors



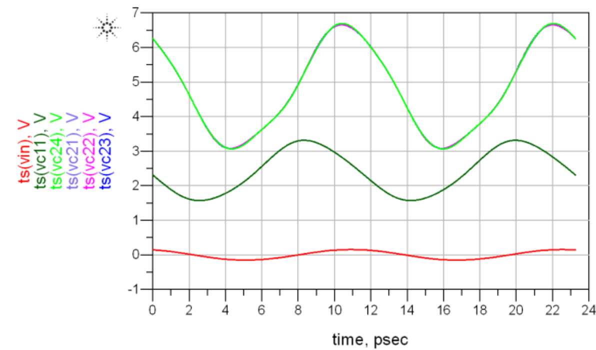
two-stack 4-finger transistors





Pin	Pout	Gain
11.000	18.125	7.125

[dBm]



Pin	Pout	Gain
3.000	16.305	13.305

[dBm]

Future work

- Further optimization of two-stack power cells
- Implementation of three- and four-stack power cells
- Investigation on efficient topologies for impedance matching
- Parallel combination of multiple power cells
  (e.g. Wilkinson, baluns...)

Thank you!