75 GHz InP DHBT Power Amplifier Based on Two-Stacked Transistors

Michele Squartecchia [#1], Virginio Midili [#], Tom K. Johansen [#], Jean-Yves Dupuy [*], Virginie Nodjiadjim [*], Muriel Riet [*], Agnieszka Konczykowska [*]
[#] *Department of Electrical Engineering, Technical University of Denmark*
348 Ørsted Plads, 2800 Kongens Lyngby, Denmark
[1]micsqua@elektro.dtu.dk
[*]*III-V Lab (joint lab of Nokia Bell Labs, Thales, and CEA-Leti)*
1 avenue Augustine Fresnel, F-91767, Palaiseau Cedex, France

***Abstract*—In this paper we present the design and measurements of a two-stage 75-GHz InP Double Heterojunction Bipolar Transistor (DHBT) power amplifier (PA). An optimized two-stacked transistor power cell has been designed, which represents the building block in the power stage as well as in the driver stage of the power amplifier. Besides the series voltage addition of the stacked structure, parallel power combining techniques were adopted to increase the output power of the MMIC amplifier, with four-way and eight-way corporate power combiners at the driver and power stages, respectively. At 75 GHz, the power amplifier exhibits a small signal gain of $G = 12.6$ dB, output power at 1-dB compression of $P_{out,1dB} = 18.6$ dBm and a saturated output power of $P_{sat} > 21.4$ dBm.**

***Keywords*—Indium phosphide; double heterojunction bipolar transistor (DHBT); power amplifier; stacked transistor; power combining.**

I. Introduction

The E-band frequency range is well suited for applications like backhaul wireless communications (71-76 GHz and 81-86 GHz), automotive radars (77 GHz), imaging (94 GHz), and many others. In such systems, power amplifiers design and optimization are of paramount importance for reliable signal transmission. To operate at these frequencies, semiconductor devices have been heavily downscaled for achieving high values of f_T and f_{max} [1]. The downside of this trend is the subsequent reduction of the breakdown voltage and output power. Many efforts have been deployed to overcome this drawback and the most widespread solution is the stacked-transistor topology, consisting of two or more transistors connected in series in a cascode-like configuration [2]-[4]. In this way the overall output voltage swing can be significantly increased as it is shared equally among the transistors. The main difference with respect to the standard cascode is that the base (or gate) terminal of the common-base stage is connected to ground through a finite impedance (typically a capacitance) which plays an important role for interstage matching and makes the base (or gate) voltage oscillate together with the collector (or drain), preventing voltage breakdown. Another beneficial outcome of the stacked topology is an increased optimum load impedance, which results in a smaller transformation ratio of the matching network improving the overall power amplifier efficiency. This is an important aspect to consider also for low loss parallel power combining as a mean to increase the output power [5].

So far, the stacked-transistor topology has been widely investigated on silicon-based devices due to their limited breakdown voltage, especially for CMOS transistors [6]. This work represents an attempt to extend the concept to InP DHBTs. We propose a 75-GHz two-stage InP DHBT MMIC power amplifier using optimized two-stacked transistors as basic power cells. In the power stage, they are combined in parallel by means of an eight-way corporate power combiner implemented with coplanar waveguides (CPW). The same power cells are used in the driver stage in a four-way parallel combined topology. The InP DHBT technology used in this design is briefly described in Section II. In Section III, the main features of the power cell and the full MMIC design are illustrated. In Section IV, measurements results in small and large signal regimes are reported. Conclusions and comments follow in Section V.

II. InP DHBT Technology

The InP DHBT technology employed in this design is optimized for high speed mixed-signal ICs and has been developed at III-V Lab [7]. Four-finger transistors featuring total active area of $4\times0.7\times10\ \mu m^2$, breakdown voltage BV_{ceo}=4.75 V and f_T/f_{max}=340/370 GHz are used in the power cells. A modified UCSD HBT model extracted from previous measurements is used in simulations to predict their behavior [8]. Passive devices and interconnects are realized on a three-layer stack process (met1-met3). It comprises 40Ω/□ NiCr resistors and 0.49 fF/µm^2 Si_3N_4 MIM capacitors. Power combining, matching networks and bias lines are realized in CPW using PtTiAu metallization.

III. Circuit Design

A. Power cell

The schematic of the two-stacked transistor power cell is shown in Fig. 1a, where Q_1 and Q_2 represent the four-finger DHBT devices. At the base input of the common-emitter stage, the parallel R_1-C_1 is inserted for stabilizing the power cell at low frequencies. Besides stabilization, R_1 is also part of the base bias network (omitted in the Figure). The two transistors

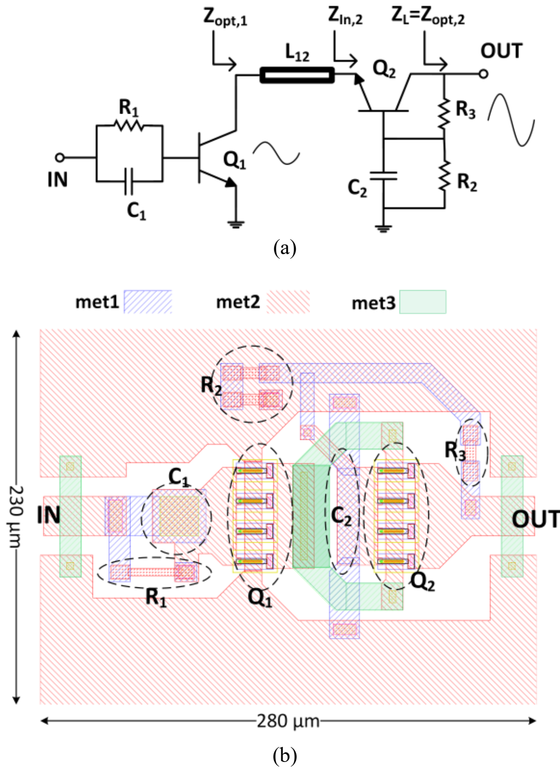

Fig. 1. Two-stacked transistor power cell: (a) schematic view and (b) layout view (bias network omitted).

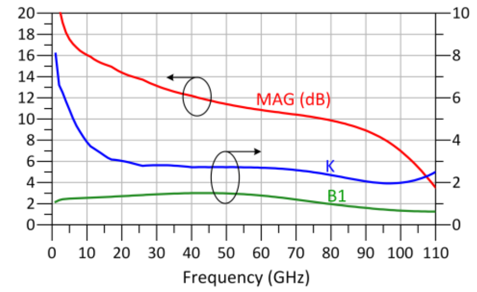

Fig. 2. Simulated Maximum Available Gain (MAG), stability factor K and stability meausre $B1$ of the two-stacked transistor power cell

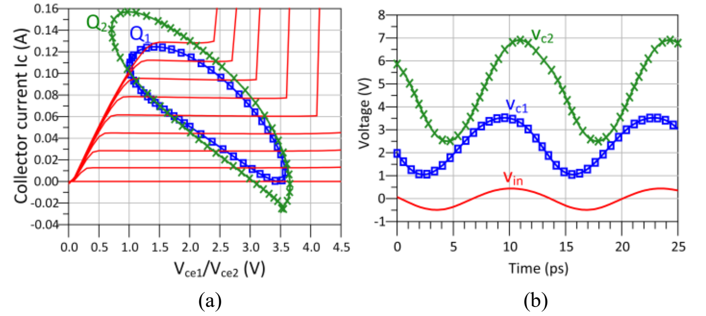

Fig. 3. Simulated dynamic load-line (a) and voltage waveforms (b) taken at the collector nodes of Q_1 and Q_2 with saturated output power P_{sat}=18 dBm and Z_L=$Z_{opt,2}$=14+j8 Ω at 75 GHz.

are biased for Class A operation and such that V_{ce1}=V_{ce2}=2.4 V, with a DC collector current of I_c=60 mA. This is accomplished by means of a self-bias resistive voltage divider R_2-R_3. The first step in the design process of the stacked-transistor is a load-pull simulation test for the determination of the optimum load impendance $Z_{opt,1}$ of Q_1. For optimum power transfer, the input impedance of the common-base stage $Z_{in,2}$ should be matched to this value. An approximated analytical formula for calculating $Z_{in,2}$ is given in [9], where its dependence on the base capacitance C_2 and output load Z_L is proved. C_2 and Z_L determine also the magnitude and phase of the RF output voltage, which should satisfy the principal objective of the stacked transistor, that is in-phase voltage addition. A straightforward procedure to find C_2 and Z_L is reported in [10]. Besides self-bias, the role of the feedback network R_2-R_3 is to stabilize the power cell at all frequencies and their values are chosen in such a way that the output power and gain are only negligibly affected. The interconnection of finite length between the two transistors is modeled in the schematic by the transmission line L_{12}, which plays a role also for interstage impedance matching. The layout of the stacked power cell is shown in Fig. 1b, where the single components are highlighted. Their values have been chosen after an iterated optimization process based on EM-circuit co-simulations carried out on ADS Momentum. In Table I, those values are summarized.

TABLE I. CIRCUIT PARAMETERS' VALUES

R_1	C_1	C_2	R_2	R_3
250 Ω	300 fF	80 fF	130 Ω	60 Ω

From the simulated small signal characteristics reported in Fig. 2, it can be seen that the power cell is unconditionally stable at all frequencies, with a maximum available gain (MAG) of 10 dB at 75 GHz. To evaluate its performance in large signal regime, it is useful to examine the dynamic load-line (Fig. 3a) and the time-domain voltage waveforms (Fig. 3b) taken at the collector nodes of Q_1 and Q_2 when the power cell is operating in saturation and with a load impedance Z_L=$Z_{opt,2}$=14+j8 Ω. The simulated voltage and current swings are within the safe operating area (SOA) and the output power is P_{sat}=18 dBm. There is a small phase misalignment between the two voltage waveforms v_{ce1} and v_{ce2} introduced by the finite interconnection L_{12}. This phase-shift, however, does not harm the reliability of the power cell, as the breakdown voltage is never exceeded.

B. MMIC Power Amplifier

The schematic representation of the two-stage InP DHBT power amplifier is shown in Fig. 4a. The power stage is composed of eight power cells combined in parallel by means of a corporate combiner implemented in CPW technology with characteristic impedance Z_0=50 Ω. The four-way combined driver stage has been implemented with the same principle. To suppress all odd-mode instabilities, 10-Ω resistors have been placed midway between adjacent power cells so the even mode is not affected. Bias networks are realized with quarter-wavelength stubs dynamically shorted by shunt capacitors. For dc decoupling and to suppress low frequency oscillations, RC series are placed close to the bias pads. A microphotograph of

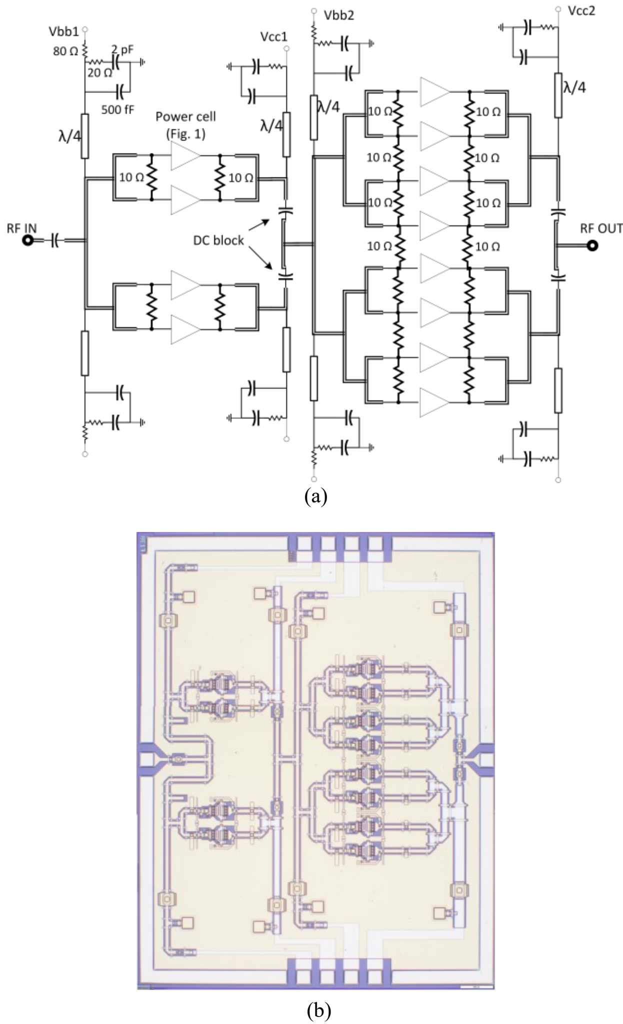

Fig. 4. Schematic representation (a) and chip microphotograph (b) of the two-stage InP DHBT power amplifier. The MMIC size is is 2.4×3.0 mm^2.

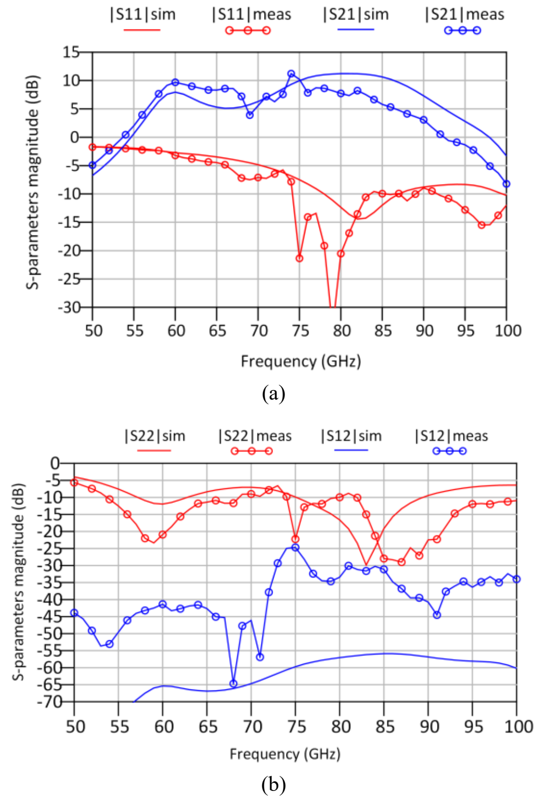

Fig. 5 Simulated (solid line) and measured (solid line with symbols) S-parameters of the designed power amplifier.

the InP DHBT power amplifier is shown in Fig. 4b. The MMIC size is 2.4×3.0 mm^2.

IV. Experimental Results

A. S-parameters

Power amplifier characterization has been carried out on wafer with RF GSG probes. S-parameters have been measured with an Anritsu VNA MS4647. In Fig. 5, measured S-parameters are compared with EM-circuit co-simulation results obtained on Keysight ADS. It can be seen that the measured data are slightly down-shifted in frequency with respect to simulations. The measured input return loss (Fig. 5a) is comparable with the simulated one and it is even higher between 75 GHz and 81 GHz, being better than 15 dB. The maximum measured gain is 11 dB at 74 GHz. The same value was obtained in simulation at 81 GHz. In Fig. 5b, the output return loss and the reverse isolation are shown. The latter is better than 25 dB at all frequencies.

B. Large signal measurements

The large signal behavior of the InP DHBT power amplifier has been measured at 75 GHz with a custom-made setup illustrated in Fig. 6. The sinusoidal signal source at 12.5 GHz is generated by the frequency synthesizer 68169B by Anritsu. The required 75-GHz signal is then obtained by means of the frequency multiplier (×6) RPG AFM6, which features a maximum output power of 7 dBm. A variable attenuator 0-50 dB is used for making the power sweep possible, and the medium power amplifier (MPA) RPG 7090 is used to restore acceptable levels of power fed into the device under test (DUT). The output power level is detected by the power sensor W8486A from Agilent and measured by the power meter Agilent N1914A. After calibration, it was found that the maximum power at the input probe-tips with this setup is 12.2 dBm, not enough to bring the power amplifier under test to saturation. The maximum measured output power, not corresponding to the saturated one, is 21.4 dBm and the 1-dB compression point is 18.6 dBm. The linear power gain is 12.6 dB, which seems optimistic if compared to S-parameter measurements. The small discrepancy could be attributed to the not perfectly calibrated homemade setup. The maximum PAE resulted in a quite low 3% due to the high DC current absorbed by the power amplifier and flowing to the resistive self-bias networks. In the small signal regime, the implemented power amplifier seems to exhibit better performances than the simulated one, but

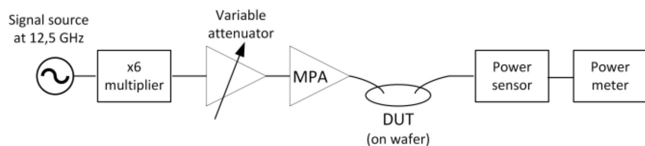

Fig. 6. Concept diagram of the large signal measurement setup at 75 GHz.

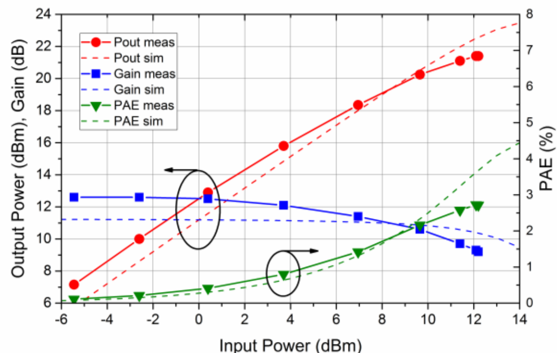

Fig. 7. Large signal characterization of the designed InP DHBT power amplifier at 75 GHz.

compression occurs earlier than predicted. Observing the output return loss in Fig. 5b, it can be inferred that, because of the frequency shift, the power amplifier is terminated with an output load slightly different from the optimum. This may be the reason for an early compression.

V. Conclusions

An InP DHBT power amplifier based on two-stacked transistors operating around 75 GHz has been designed and reported in this work. The operating principle of the basic power cell structure has been discussed. It has been optimized by EM-circuit co-simulations and its key performances have been highlighted. The power amplifier is made up of two stages: an eight-way combined power stage driven by a four-way combined driver stage. Power combination is realized with low loss corporate architectures implemented with CPW lines. Despite the fact that the transistors were optimized for high-speed mixed-signal applications, more than 21 dBm of output power and 12.6 dB of linear power gain have been obtained. Higher performances are expected from a power-optimized process currently underway. Moreover, a dedicated large signal measurement setup will allow the power amplifier to be fully saturated.

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