Low Conversion Loss 94 GHz and 188 GHz Doublers in InP DHBT Technology

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***Abstract*—An Indium Phosphide (InP) Double Heterojunction Bipolar Transistor (DHBT) process has been utilized to design two doublers to cover the 94 GHz and 188 GHz bands. The 94 GHz doubler employs 4-finger DHBTs and provides conversion loss of 2 dB. A maximum output power of nearly 3 dBm is measured while the doubler is not entirely saturated. The DC power consumption is 132 mW. The 188 GHz doubler utilizes a 1-finger DHBT. Conversion loss of 2 dB and a maximum output power of -1 dBm are achieved at 188 GHz with on-wafer measurements. The DC power consumption is 24 mW under saturated conditions. Both doublers operate over a broad bandwidth. The total circuit area of each chip is 1.41 mm^2.**

Keywords—frequency doubler, frequency multiplier, heterojunction bipolar transistor, indium phosphide, millimeter-wave monolithic integrated circuits.

I. Introduction

The availability of fundamental tone sources in the millimeter-wave range is limited, which makes frequency multipliers an essential component in systems employing millimeter-wave signals. One of the examples is dynamic nuclear polarization (DNP) systems, where polarization efficiency relies on availability of millimeter-wave radiation [1]. This work presents a family of doublers covering frequency bands which are of interest for 3.35 T and 6.7 T DNP systems [2] and is a first step towards partially integrating millimeter-wave sources into DNP cavities. The circuits are designed for low insertion loss and fabricated in a high-speed InP DHBT circuit technology [3] developed at III-V Lab. The following two Sections of the paper provide a description of the circuit design as well as measurement data.

II. 94 GHz Doubler

A. Circuit Design

The circuit is based on a single-ended topology and utilizes a single 4-finger DHBT. For optimum power conversion the input of the transistor is matched at the fundamental frequency while the output is matched at the second harmonic. The output circuit also suppresses the fundamental frequency signal in the load by presenting short-circuit to the output of the transistor at this frequency. The same is done at the input of the transistor for the second harmonic. The matching circuits are realized using open-circuited and short-circuited stubs. AC coupling MIM capacitors are used to provide RF ground for short-circuited stubs. The layout is based on coplanar waveguide (CPW) transmission lines, as can be seen in Fig. 1.

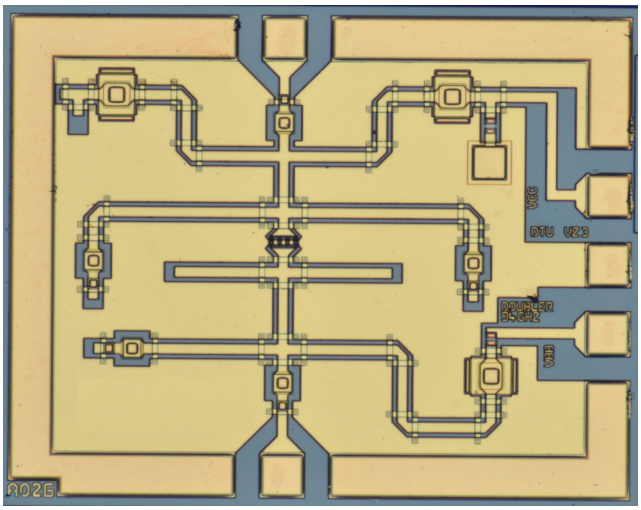

Fig. 1. Photograph of a 94 GHz doubler chip. Chip size ≈ 1.35 mm × 1.05 mm. The input is at the bottom, the output is at the top, DC pads are on the right side.

For compact layout lengthy CPW had to be bent introducing discontinuities resulting in increase of the insertion loss of the circuit by several dB. To minimize discontinuity airbridges are used at transmission line junctions to suppress undesired slot mode excitation. Another challenge in CPW based layout is truncated ground plane, which is also significantly segmented by numerous stubs. Segmented ground plane with fragments comparable to wavelength will excite parasitic modes in the circuits degrading performance of the matching and filtering circuits. Analysis of these modes can only be performed by full-wave simulations, which dramatically complicates the layout development. For reference, the guided wavelength on implemented CPW is ≈ 1.4 mm at 94 GHz, which is comparable to the chip dimensions (1.35 mm × 1.05 mm). Therefore, parasitic modes should be carefully analyzed and suppressed.

The design and nonlinear analysis are performed using in-house developed models [4], Harmonic Balance implemented

in a commercially available CAD program with Method-of-Moments based EM co-simulations.

In addition to optimized conversion loss, the doubler is also designed such, that it can be used to drive a 188 GHz frequency doubler.

B. Measurements and simulations

All the measurements presented here are performed on-wafer. There was a limited availability of driving sources in the given frequency band, therefor the presented measurement data is supported by simulations, where it is relevant. The measured and simulated gain of the doubler as a function of input power for a range of frequencies is shown in Fig. 2.

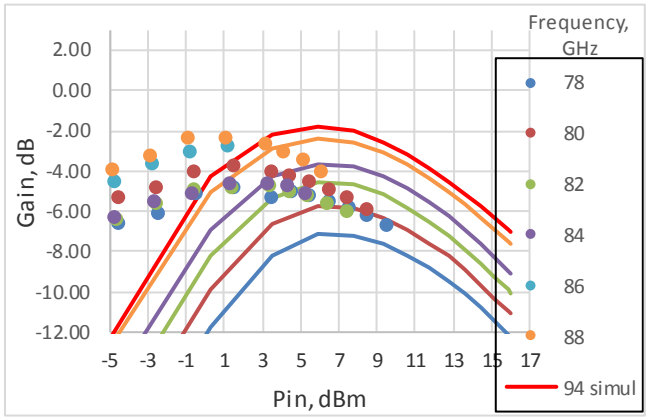

Fig. 2. Gain versus frequency for a 94 GHz doubler. Lines – simulations, markers – measurements. Colors correspond to different frequencies.

With the limitations of the current measurement setup, it is not possible to measure the circuit exactly at 94 GHz, however, the measured insertion loss at the closest possible frequency, 88 GHz, is 2 dB. Though the level of the maximum insertion loss approximately corresponds to the simulated values, the transistor reaches saturation earlier, than expected.

The measured and simulated output power of the doubler as a function of frequency and input power are shown in Fig. 3 and Fig. 4 correspondingly.

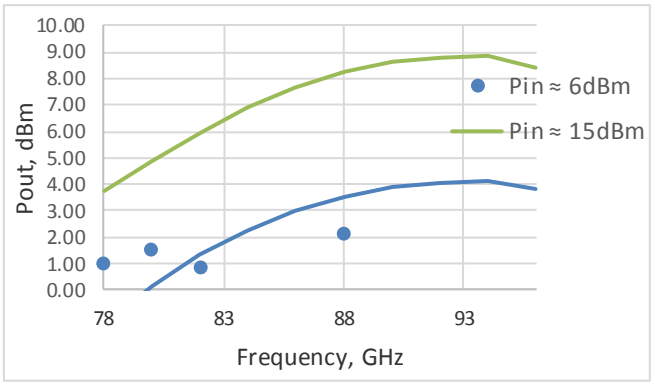

Fig. 3. Bandwidth of the 94 GHz doubler. Lines – simulations, markers – measurements. Colors correspond to different frequencies.

With the available signal sources, it was not possible to saturate the doubler completely, and the maximum measured output power reached 2.7 dBm. The bias point was constant throughout the measurement with a collector voltage of 2.4 V.

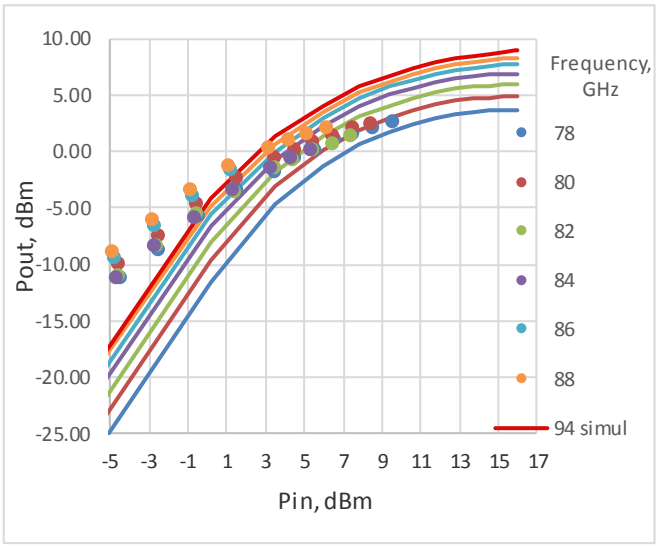

Fig. 4. Output power versus input power for 94 GHz doubler. Lines – simulations, markers – measurements. Colors correspond to frequencies.

The measured suppression of the fundamental frequency at 88/2 GHz is better than 11 dB using the available driving source.

III. 188 GHz Doubler

A. Circuit Design

The 188 GHz circuit utilizes a 1-finger DHBT having $f_T / f_{max} = 330$ GHz / 420 GHz [5]. Following the same approach as for the 94 GHz doubler, the circuit is designed and layout is developed, as shown in Fig. 5.

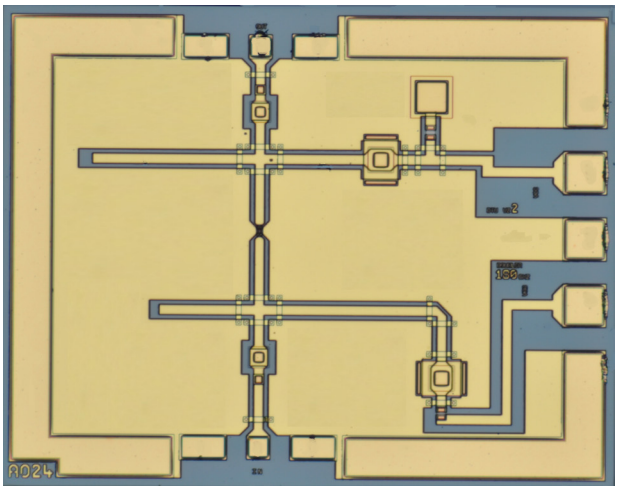

Fig. 5. Photograph of a 188 GHz chip. Chip size ≈ 1.35 mm × 1.05 mm. The input is at the bottom, the output is at the top, DC pads are on the right side.

As can be seen from the photograph of the chip, the matching and filtering circuits at the input and output are

simpler than 94 GHz design. This is due to a tradeoff between optimal matching/filtering and insertion loss. Ideally, higher order circuits provide better filtering, however, in practice, they introduce more loss.

B. *Measurements*

Method-of-Moments based EM co-simulations still provide reasonable accuracy in this frequency range. Simulations, though, are omitted in the results presented below to keep the clarity of the pictures. The measured gain of the doubler as a function of input power for a range of frequencies is shown in Fig. 6.

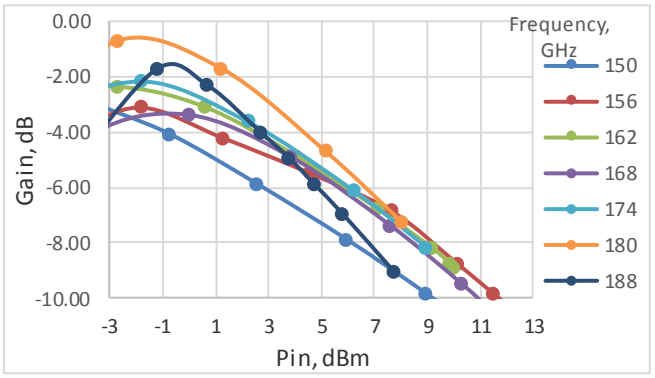

Fig. 6. Measured gain versus frequency for a 188 GHz doubler. The maximum gain is achieved for Pin in the range from -3 dBm to 1 dBm.

The minimum measured conversion loss is 0.7 dB at 180 GHz and 1.7 dB at 188 GHz with an output power of -3.4 dBm and -2.9 dBm correspondingly (refer to Fig. 7).

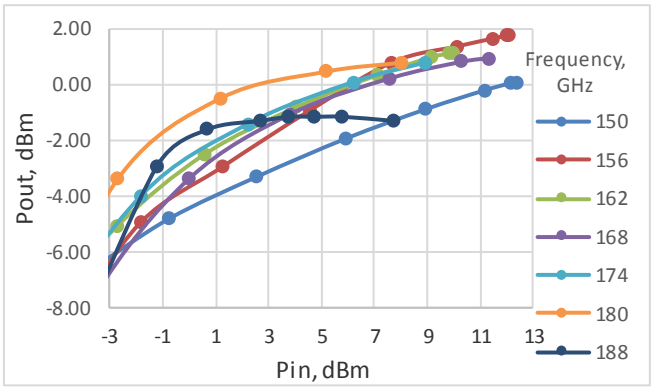

Fig. 7. Measured output power versus input power for 188 GHz doubler. At 188GHz the doubler reaches saturation at Pin ≈ 1 dBm.

The bias point is constant throughout the measurement with a collector voltage of 2.4 V. The collector current in saturation is approximately 10 mA.

Further increasing driving level a maximum output power of -1.1 dBm could be achieved at 188GHz, which is the upper boundary of the operating frequency band, as can be seen in Fig. 8. At maximum drive the doubler demonstrates fairly constant output power in the entire measured frequency range from 150 GHz to 188 GHz.

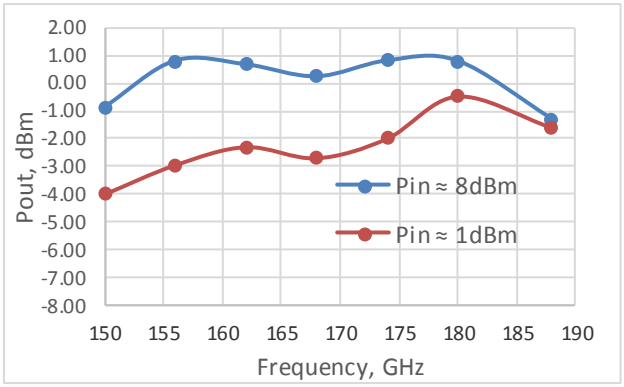

Fig. 8. Measured bandwidth of the 188 GHz doubler.

The measured suppression of the fundamental frequency is better than 11 dB.

IV. Conclusions

A family of single-ended 94 GHz and 188 GHz frequency doublers is designed and fabricated. The circuits are based on InP DHBT devices and CPW technology. Though CPW itself provides good performance in millimeter-wave range, layout development for circuits relying on CPW components with distributed parameters is proved to be challenging. Nevertheless, the measured results on the fabricated doublers demonstrate low conversion loss at low input power and good suppression of the fundamental frequency component.

Acknowledgment

The authors would like to thank European Commission (FP7-People-2013-ITN IN-POWER, grant #607647) for partial support of the activities.

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