Electrical and Thermal Characterization of Single and Multi-Finger InP DHBTs

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***Abstract*—This paper presents the characterization of single and multi-finger Indium Phosphide Double Heterojunction Bipolar transistors (InP DHBTs). It is used as the starting point for technology optimization. Safe Operating Area (SOA) and small signal AC parameters are investigated along with thermal characteristics. The results are presented comparing different device dimensions and number of fingers. This work gives directions towards further optimization of geometrical parameters and reduction of thermal effects.**

I. Introduction

InP DHBTs are currently one of the major technologies for millimeter-wave wireless applications. Due to their excellent power handling capabilities and high operating frequencies, they are regularly employed in power amplifiers (PA) MMIC applications. Recent results demonstrated circuit topologies with a high output power of 180 mW at 214 GHz [1].

The advancements in circuit applications rely on continuous improvements and optimization of existing transistor technologies. The starting point on the path to a fully optimized device is the characterization of present technology and the extraction of relevant device parameters. For PA applications, breakdown voltage and safe operating area (SOA) are important DC characteristics to improve for maximum operating swing of the amplifier [2]. Maximum oscillation frequency is also typically determined during electrical characterization because it is an important figure of merit to predict transistor performances for analog circuits. Starting from single finger devices, multi-finger structures are realized to deliver an increased output power. Multi-finger DHBTs are normally operated at higher power dissipation and the additional heat generation degrades the overall device performances and characteristics. Thermal properties of the devices are to be determined to deal with self-heating and additional effects such as thermal coupling between the fingers.

The results in this work present a comparison of the impact of the different geometrical parameters on device electrical and thermal characteristics. The paper is divided in three sections. In the first section the structure and the geometry of the device are briefly described. In the second section the results from electrical characterization are presented, concerning DC characteristics and AC parameters. Finally, the last section presents the results from electro-thermal characterization, including the calculation of thermal-electric feedback coefficient and the extraction of thermal resistance.

II. Device description

The DHBTs presented in this work were realized at Alcatel-Lucent Bell Labs III-V Lab. The epitaxial layers were grown by GSMBE on a semi insulating Fe-doped InP substrate and then a triple mesa self-aligned process was used. The epitaxial structure includes a 40 nm InP emitter, a 28 nm InGaAs base and a 190 nm compositional graded InP collector. Single finger and multi-finger devices were realized with three different emitter lengths $\mathrm{L_E}$: 5, 7 and 10 μm. For single finger transistors, devices with different emitter width $\mathrm{W_E}$ 0.5, 0.7, 1, 1.5 μm, were compared. Multi-finger devices in this investigation have 2-3-4-6-8 equally spaced single-transistors fingers in a parallel structure.

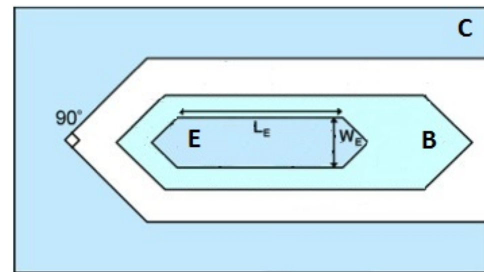

Fig. 1. Schematic top view of single finger DHBT. Emitter length is referred to as $\mathrm{L_E}$ and emitter width as $\mathrm{W_E}$. Emitter, base and collector contacts are indicated as E, B, C.

III. Electrical characterization

A. DC characteristics

Static measurements were performed to determine the large signal behavior of the device. Gummel plots and $\mathrm{I_c}$-$\mathrm{V_{ce}}$ curves were measured to assess correct behaviour and compare static performance metrics such as forward current gain and collector current level. The value of forward current gain β is reported to be in the range 34-40 both for single-finger and multi-finger transistors. Characteristic curves showed to be consistent with scaling of device dimensions and geometries. The SOA of the devices was determined measuring collector current $\mathrm{I_c}$ for increasingly higher collector emitter voltages at different constant base current values ranging from 0 to 2 mA with a 0.2 mA step. In many cases, this process leads to a sudden device failure so data are taken from transistors of the same kind fabricated on different sites across the wafer. Fig.2 present the measurement results of SOA characterization of a 4 fingers DHBT with an active emitter area of $4 \times 10 \times 0.7 \mu\mathrm{m}^2$. The breakdown voltage seems to be larger than 6V. In order to

determine SOA boundary points plot of Fig.2, two distinct failure behaviors can be observed on the plot as explained in [2]. For high voltages and low values of base current I_b close to 0, I_c increases continuously before device failure occurs. This behavior follows a typical breakdown mechanism that can be attributed to impact ionization in the collector at high electric fields. For curves at higher base current, collector current remains flat and then abruptly increase. This is due to increased junction temperature which leads to device failure. The exact mechanism of failure in this region, however, is not yet fully understood but it seems to be related to base-emitter junction periphery and emitter sidewalls.

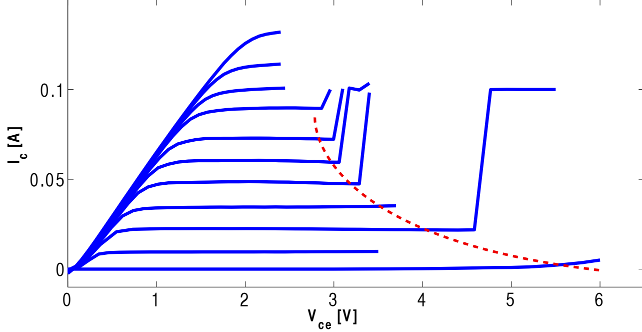

Fig. 2. SOA measurement results of a 4-finger DHBT. Emitter area per finger is 10x0.7μm^2. I_c is measured as a function of V_{ce} almost until device failure for different I_b values. Base current is increased in the range 0-2 mA with 0.2 mA step.

B. Small signal parameters

S-parameters measurements were performed to determine the parameters of devices small-signal model (Fig. 3) and the frequency performances in terms of cutoff frequency f_T and maximum oscillation frequency f_{max}.

S-parameters measurements were carried out from 250

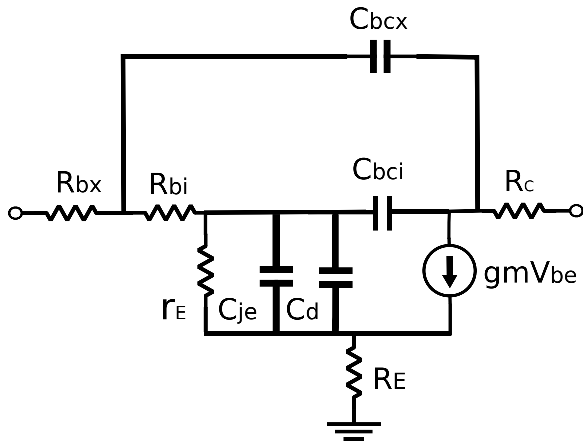

Fig. 3. Small signal model of a DHBT.

MHz to 110 GHz for single finger and multi-finger devices. Transistors were measured at different bias points while setting collector-emitter V_{ce}voltage at 2.4 V. Firstly, cut-off frequency f_T is presented as a function of emitter length L_E. f_T is dependent on device geometry and on the product of different small-signal parameters as can be seen in Eq. (1) :

$$\frac{1}{2\pi f_T} = \tau_b + \tau_c + r_E(C_{je} + C_{bc}) + (R_E + R_C)C_{bc} \quad (1)$$

where τ_b and τ_c are base and collector transit time respectively, $r_E = kT/qI_c$ is the inverse of small-signal transconductance, C_{je} is the junction capacitance, C_{bc} is the total collector capacitance and R_E and R_C are the parasitic emitter and collector resistances.

Device f_{max} is affected by the distributed R_b-C_{bc} product and f_T value according to Eq. (2):

$$f_{max} \sim \sqrt{\frac{f_T}{8\pi(R_{bx}(C_{bcx} + C_{bci}) + R_{bi}C_{bci})}} \quad (2)$$

where R_{bi}-R_{bx} and C_{bci} and C_{bcx} are the intrinsic and extrinsic resistances and collector-base capacitances, respectively. Starting from de-embedded measurement data, device small-signal current gain H_{21} and Mason's unilateral power gain U can be plotted versus frequency. f_T and f_{max} are extrapolated by fitting -20dB/decade line to experimental data.

Fig.(4) presents values of f_T of single finger transistors having emitter length from 5 to 10 μm and emitter width from 0.5 to 1.5 μm . Reported f_T and f_{max} values refer always to the frequency peak value reached by increasing collector current I_c at $V_{ce} = 2.4V$ before a drop off due to Kirk effect. The emitter resistance and base-emitter capacitance have opposite trends with respect to total active area variations. As expected from theory, cutoff frequency decreases at most with 10% variation with respect to device geometrical scaling and is only slightly larger for devices with smaller emitter width.

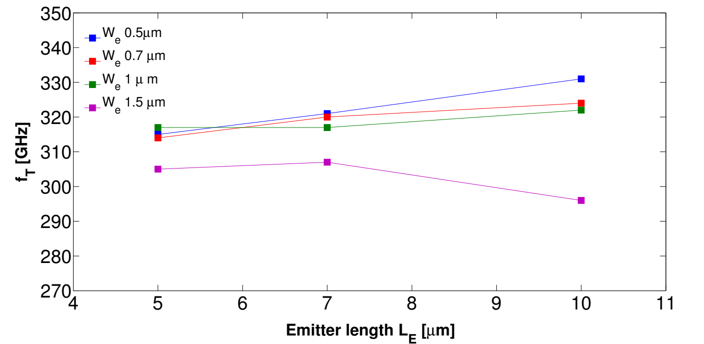

Fig. 4. Cutoff frequency f_T extracted from measurement as a function of L_e for devices with different emitter width W_e from 0.5 to 1.5 μm

Fig.5 presents the results for f_T of a set of multi-finger transistors with emitter length values in the range 5 - 10 μm. In this case emitter width was constant for all devices at 0.7 μm. Cutoff frequency f_T presents a 10% maximum decrease with increasing emitter length for a given device. As expected, f_T does not depend strongly on geometrical layout dimensions, at least for small number of fingers. f_T peak values decrease as the number of fingers increases, going from 320 GHz for 2 fingers down to 270 GHz for an 8 finger device. This effect can be explained in part by the junction temperature increase with increasing dimensions that might be responsible of a reduced average carrier velocity.

Measurement results in Fig. 6 show that f_{max} peak values in

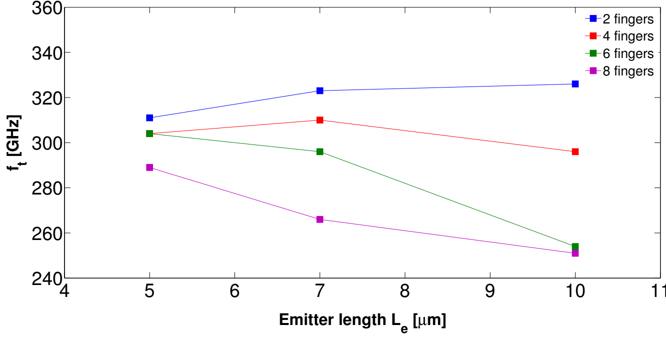

Fig. 5. Extrapolation of f_T as a function of emitter length L_e from measured data for multi-finger devices.

general decrease for increasing emitter length. This behavior has been explained taking into account the phenomenon for which longer emitter transistors may have a high base contact resistance because the area participating to conduction is actually reduced.

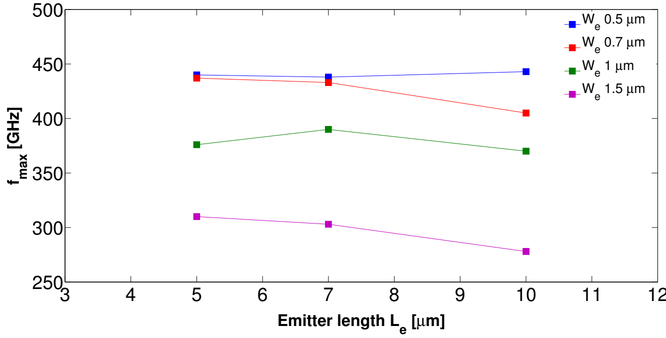

Fig. 6. Maximum oscillating frequency f_{max} as a function of L_e

Fig. 7 shows the variation of f_{max} with emitter length for multi-finger DHBTs. The peak value reported for 2-fingers devices is 450 GHz and for 8 fingers is around 370 GHz. The maximum oscillating frequency decrease with increasing emitter length becomes more visible. In addition, it also steadily decreases when the number of fingers goes from 2 to 8. Two concurrent effect can explain this tendency. The first is the increased junction temperature at a higher number of fingers that is responsible of the reduction of the average carriers velocity, leading to an increased base-collector transit time τ_{cb}. The second effect is the presence of inter-finger parasitics, especially the external emitter inductance, that become relevant with a high number of fingers.

IV. Thermal-Electric Characterization

A. Thermal-electric feedback coefficient

Every bipolar device exhibits the property that the base-emitter voltage V_{be} required to reach a defined current density J_c, decreases at higher junction temperatures. The thermal-electric feedback coefficient takes this effects into account and

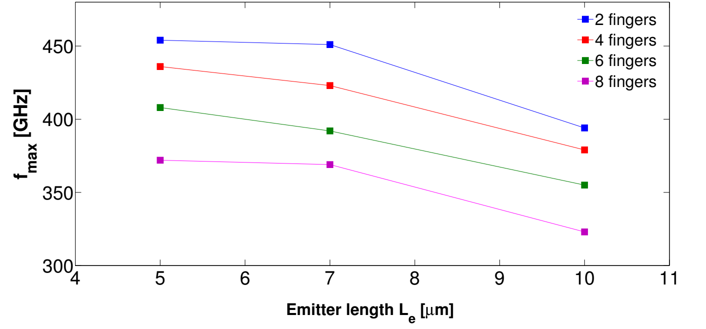

Fig. 7. f_{max} as a function of L_e for multi-finger devices having 2-4-6-8 fingers.

is defined as

$$\phi = -\frac{\partial V_{be}}{\partial T} = \frac{\beta^*}{q} - \frac{\eta k}{q} \ln \frac{I_C}{I_{s_0}} \tag{3}$$

where β^* is the band gap shrinking coefficient, η is the ideality factor and I_{s_0} is the saturation current at room temperature. Based on the approach from [3], the ϕ coefficient was computed from I_c and V_{be} measurements on a single finger transistor. Collector current I_c is plotted as a function of base emitter voltage V_{be} at different temperature values. Measurements were performed at temperature T equal to 20°,40°,60°,80°C. For a given I_c value, the corresponding V_{be} is extracted and plotted against temperature. The I_c values used to extract the ϕ coefficient are 5, 10, and 15 mA as for these values the collector current of the single finger device of area $5 \times 0.7 \mu m^2$ has still an exponential relationship with the base-emitter voltage. Fig. 8 shows the relationship between V_{be} and temperature. The required V_{be} voltage to provide a given current density decreases with increasing temperature. In the rest of this work, the ϕ coefficient is considered constant across the wafer (within standard deviation of epitaxial layers fabrication process) so the same value was employed in the case of single and multi-finger devices. The thermal-electric

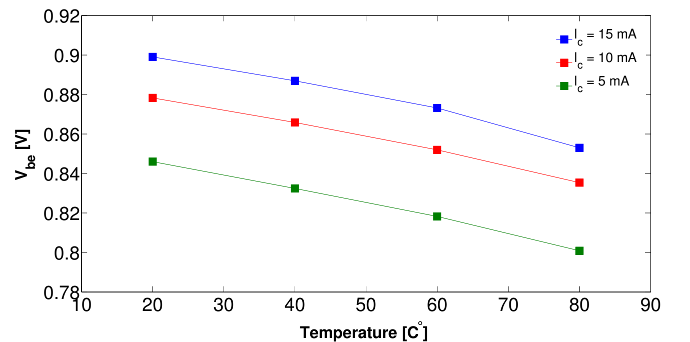

Fig. 8. Base-emitter voltage V_{be} as a function of temperature T at different current densities. Data points are fitted with a straight line and the slope is the thermal electric feedback coefficient

feedback coefficient is dependent on device current density as shown in Fig.9 and the slope of the fitted straight line in logarithmic scale is approximately equal to the theoretical value $-\eta K/q$ as predicted in Eq. 3.

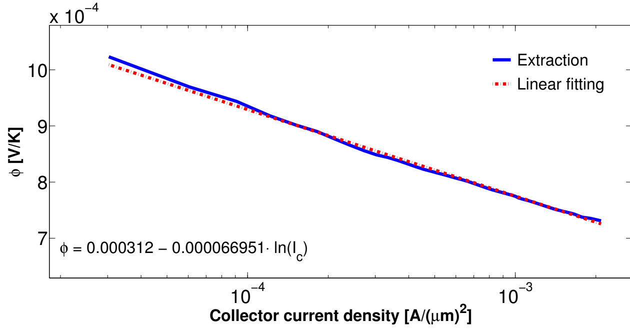

Fig. 9. Thermal electric feedback coefficient ϕ as a function of collector current density J_c for a single finger device of area $5 \times 0.7 \mu m^2$. The extracted coefficient was fitted with a straight line (shown in red)

B. Thermal resistance

The parameter that mostly affects transistor thermal properties is the self-heating thermal resistance R_{th}. As power dissipation increase at high current densities, a large value of thermal resistance is responsible for high increase in junction temperature: this in turn leads to variations in other device parameters and to a potential failure. For a multi-finger device an additional mutual thermal resistance exists among the fingers. Total thermal resistance values for single and multi-finger devices were computed according to:

$$R_{th} = \frac{\Delta V_{be}}{\Delta P \phi} = \frac{\Delta V_{be}}{\Delta V_{ce} I_c \phi} \quad (4)$$

In the case of multi-finger transistors, the result from Eq. (4) represents a total thermal resistance that includes mutual heating effects among the fingers. For the DHBTs in this work, thermal resistance values were determined from measurements as follows. For every device, first collector current I_c was measured as a function of V_{be} at different collector-emitter voltage V_{ce} ranging from 0.9 to 2.4 V. For a given I_c value,

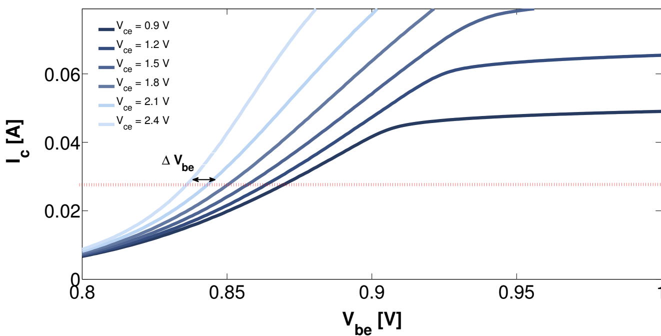

Fig. 10. Measured collector current I_c as a function of V_{be} for a 2-finger device of area $2 \times 10 \times 0.7 \mu m^2$. The horizontal line represents a given current value at which ΔV_{be} is extracted as the difference between two adjacent curves.

the variation in base-emitter voltage ΔV_{be} as the distance between the curves, as shown in Fig.10. The increase in dissipated power is constant between each curve and equal to $\Delta P = \Delta V_{ce} \times I_c$. Inserting ΔV_{be}, the coefficient ϕ and ΔP in Eq. 4 allows to compute thermal resistance values for each transistor for different values of dissipated power. Thermal resistance varies non-linearly with the number of fingers and ranges from 3500 to 1900 C°/W for single finger devices with area of 5x0.7 and 10x0.7 μm^2, respectively. Starting from thermal resistance at a constant power density, specific thermal resistance for unit area was computed and results are presented in Fig.11. Specific thermal resistance increases with the number of finger because of additional mutual heating effects. In addition, total specific thermal resistance increases with L_e and an increasing spreading between the curves can be observed for higher number of fingers. This tendency could be due to different heat distribution across the same finger for devices with different emitter lengths: devices with longer emitter might have a larger thermal resistance because of a higher increase in temperature for a constant power density.

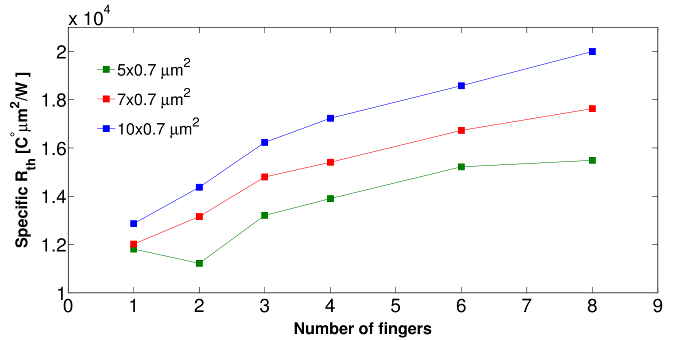

Fig. 11. Specific thermal resistance R_{th} as a function of the number of fingers for 5,7,10 μm emitter lengths. R_{th} was computed at a constant power density with $J_c = 1 \mathrm{mA}/\mu \mathrm{m}^2$ and V_{ce} = 2.4 V

V. Conclusion

Electrical and thermal properties of single finger and multi-finger InP DHBTs up to 8 fingers were investigated. SOA measurements showed a breakdown voltage greater than 6 V and highlighted the two main device failure behaviors. The AC characterization results show that both f_T and f_{max} decrease with an increasing number of finger. Electric thermal feedback coefficient was extracted and total thermal resistance was compared showing that the specific thermal resistance is higher for devices with larger emitter area and increases with the number of fingers.

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